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VLSI ARCHITECTURE FOR ENERGY DETECTION BASED SPECTRUM SENSING BY USING PARALLEL PREFIX ADDERS

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Abstract
The increase in Wireless communication and network has resulted in shortage of spectrum. In order to overcome this spectrum scarcity problem, Cognitive radio (CR) technology is used. This technology provides the way for utilization of spectrum completely by means of identifying the unused holes in the spectrum band. But the spectrum has to be sensed for identifying the available spectrum which is somewhat complicated. However the sensing of spectrum can be done by energy detection technique. Through this ED technique, complexities faced during implementation of detection process will be reduced. A newly optimized energy detection architecture has been designed, in which the area and power performance will be optimized. And another ED block with reduced delay is also implemented. To achieve better performance, in terms of area and delay, the adder is replaced with Parallel prefix adders (PPA), such as Kogge stone adder and Brent kung adder. Such energy detection based spectrum sensing has been developed by Verilog coding using XILINX ISE 14.7 software.

Keywords: Cognitive radio (CR); sensing scheme; Energy detection; spectrum utilization; ED technique; Parallel prefix adders (PPA)

I. INTRODUCTION

Today's emerging technology and devices paved the way for major demand of spectrum resource usage and it is gradually increases as the technologies grow rapidly. In order to solve this demand, the overall spectrum has to be utilized properly by all primary as well as secondary users of the wireless network .

Generally there are primary users named as licensed users and secondary users (named as unlicensed user) of a network. Sometimes the primary user part of the spectrum is not used and it is said to be white holes. Such holes will be efficiently used by assigning it to the unlicensed users in the network.

A cognitive radio (CR) can change its transmitter's parameters based on the environment in which it performs. Usually the cognitive radio technology may have software defined technique. Then in case of communication purpose between two terminals (two spectrum users) the detection process will be performed perfectly and allocate the unused one to needed node in the wireless network". Since this CR technology is implemented intelligently and can be adjustable to all the environments which may reduce the complication of spectrum sensing in over wide band. Various difficulties

has been faced while doing the detection process. And some of the confronting difficulties are listed as follows:

A. SNR value of the input sensed signal is much more important

B. Timing scattering and multipath deviation of the signal in the network.

There are numerous ways invented in order to detect the spectrum occupied by the primary users. Some of the detection techniques that used now-a-days for sensing the spectrum are Collaborative and Distributed networks and these are establishing some of the methods such as based on energy detection, matched filtering and cyclo-stationary feature detection.

Some of the features of CR are given as follows: The unlicensed user (Secondary user) leaves the spectrum at once that the licensed users access the spectrum. A spectrum sensing plays a vital role in CR technology. To distinguish the unused bands two techniques are used, one is database oriented sensing and spectrum sensing oriented method. For the most part first strategy is generally utilized in TVWS (Tele Vision White Space), in which the database contains the data about the essential users area received by FCC, as this is utilized to recognize the spectrum utilization of authorized users by getting to database. The spectrum detection is loaning the un/underutilized bit of radio spectrum from the authorized client without making obstruction Primary user. The idle frequency band can be distinguished by spectrum detection.

Now a days to avoid the high delay problem of existing adders the PPA is used which is simply the modified design form of CLA. PPA's are implemented in Very large scale Integration (VLSI) chips which rely on fast and reliable arithmetic computation, therefore PPAs are very useful in today's world of technology.

II. LITERATURE SURVEY

At first in the year of 1998, author named as Joseph Mitola newly coined the general study about cognitive radio. After that the second author who provides the elaborated study about the CR in 1999, by G. Q. Maguire.

Usually the secondary users may use the unused bands for better usage of whole spectrum. For that the spectrum holes (generally unused spectrum available in band by licensed user) has to be identified and allocated for needed user in the network. There are numerous ways to sensing the spectrum efficiently and every method has their own pros and cons.

Cyclo-Stationary based feature detection, matched filter based detection, Radio identification based sensing, Energy detector based sensing and waveform type of sensing are some of the detection techniques.

I. Cyclo stationary based detection:

It is mainly implements the concept of adding redundancies to the input. Such exploitation will be taken place by resolving the features of the signal used by licensed users in the network. It is hard to implement and takes more time for getting the desired output from it. But it performs well for low SNR value when compared to Matched filter method.

II. Matched Filter sensing Method:

It is an optimal detection technique. Improving the input SNR value is one of the advantages of matched filter detection method. But the only disadvantage of this detection technique is it needs the information about the input signal for its sensing process. It takes less computational time but complexity is more.

III. PROPOSED WORK

Energy Detection technique (ED) is a non cooperative type of detection technique .And it is one of the simplest detection techniques because of the following main reason: the information behind the input signal is not needed for detection process and hence it is named as "blind signal detector". As the name itself indicates, in this energy detection technique, spectrum can be sensed through energy calculation.

Energy detector model detects the spectrum by measuring the input signal's energy value with appropriate frequency band, and it is said to be radiometry. Calculating the energy value of the signal which is received decides whether the spectrum is used or not. The determination of the

signal's presence can be identified in the scaling unit. In such block the actual measured energy value is compared with the fixed value (named as threshold). And such fixed value is taken as reference for comparison process. Architecture of proposed Energy Detector Model is illustrated in the figure.1.

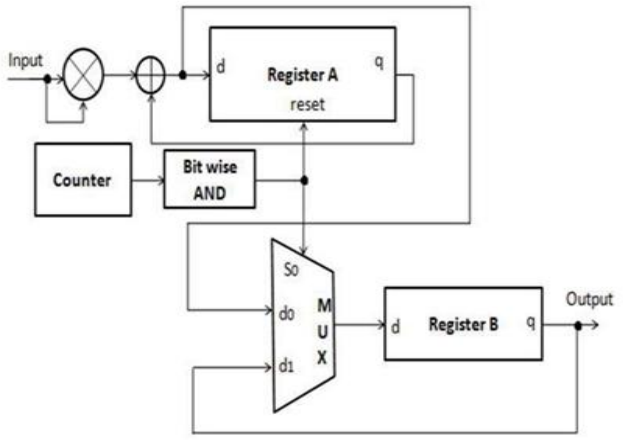

Figure 1: Proposed Energy Detector Architecture

The Architecture of optimized energy detector block is implemented based on VLSI. This Optimized Energy Detector model comprises of individual blocks such as multiplier unit (act as squaring unit), adder module (produce averaging value), scaling unit. This whole architecture is tested by providing various discrete samples of signals as an input to this detector.

At first, signal can be sampled to produce the discrete sample values. Such input samples are passed through the multiplier; here the samples are multiplied by the same samples. And thereby the squared value of the input samples can be taken out from the multiplier unit. The resulted squared samples are added by giving it to the adder circuit and accumulated using an adder–register block arrangement, as shown in Figure 1.

The accumulator unit continues its summing process of input signal and it ends when the register receives a control signal (reset) from the counter block. This summation of squared value of samples is taken as output and it is said to bean averaged output value of samples. In case of the accumulator unit, 16-bit input samples are summed up, by using register which can get the reset value from counter block. Here 16-bit counter block is used in ED architecture. By using the higher number of samples for detection purpose, it yields greater accuracy in performance.

When the input samples are of 8-bits, then it is squared to generate 16-bit values. And then counter is designed to count from 0, then it end its count value which may generate "1" by bit-wise AND block. This bit wise AND is coded to generate either "0" or "1" as an output. By means of the obtained value from bit-wise AND, Register1 is going to store a value or clear it. Multiplexer unit is used to select the signal from its two input (one is energy value of samples and another is output signal from Register2 block).Whenever the selection line of MUX is set to "1", it selects the energy value of 16samples and its output is directly applied toregister2.
Multiplexer used in the architecture is for selecting the appropriate signal by the help of its selection lines. Here 2x1MUX is used to select the adder units output and the output of register2 by applying "1" and "0" to its selection line respectively. Thereby the measured value is compared with fixed value to detect the presence of signal.

IV. RESULTS AND ANALYSIS

At the beginning, individual modules are designed independently and the entire model is collectively implemented afterwards. The proposed architecture of energy detector block is coded using a standardized hardware description language, verilog. Thereby, the presence or absence of the signal is decided.

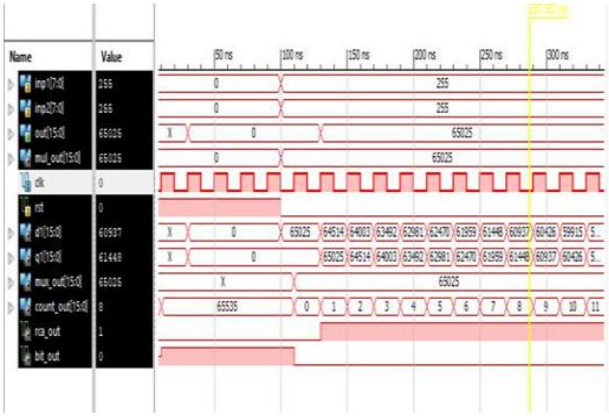

Figure 2: Simulation waveform of architecture using ripple carry array multiplier and ripple carry adder

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 7.761ns (Maximum Frequency: 128.849MHz)
   Minimum input arrival time before clock: 32.914ns
   Maximum output required time after clock: 4.394ns
   Maximum combinational path delay: No path found
```

Figure 3: Delay of architecture using ripple carry array multiplier and ripple carry adder

```
Device utilization summary:
---------------------------

Selected Device : 3s100etq144-4

 Number of Slices:                130  out of    960    13%
 Number of Slice Flip Flops:       48  out of   1920     2%
 Number of 4 input LUTs:          238  out of   1920    12%
 Number of IOs:                    34
 Number of bonded IOBs:            34  out of    108    31%
 Number of GCLKs:                   1  out of     24     4%
```

Figure 4: Area of architecture using ripple carry array multiplier and ripple carry adder

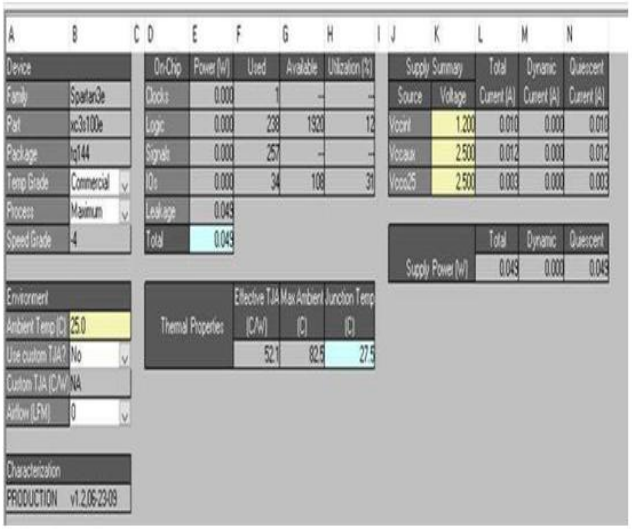

Figure 5: Power Estimation of architecture using ripple carry array multiplier and ripple carry adder

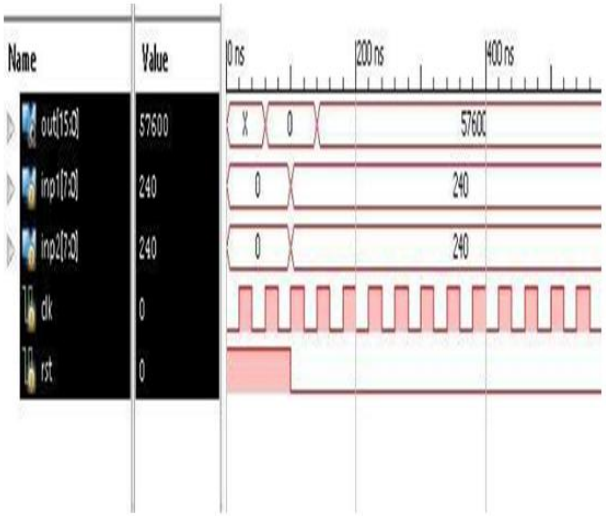

Figure 6: Simulation Waveform of architecture using ripple carry array multiplier and Kogge stine adder

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 5.307ns (Maximum Frequency: 188.430MHz)
   Minimum input arrival time before clock: 32.394ns
   Maximum output required time after clock: 4.310ns
   Maximum combinational path delay: No path found
```

Figure 7: Delay of architecture using ripple carry array multiplier and Kogge stone adder

```
Device utilization summary:
---------------------------

Selected Device : 3s100etq144-4

 Number of Slices:                114  out of    960    11%
 Number of Slice Flip Flops:       48  out of   1920     2%
 Number of 4 input LUTs:          205  out of   1920    10%
 Number of IOs:                    34
 Number of bonded IOBs:            34  out of    108    31%
 Number of GCLKs:                   1  out of     24     4%
```

Figure 8: Area of architecture using ripple carry array multiplier and Kogge stone adder

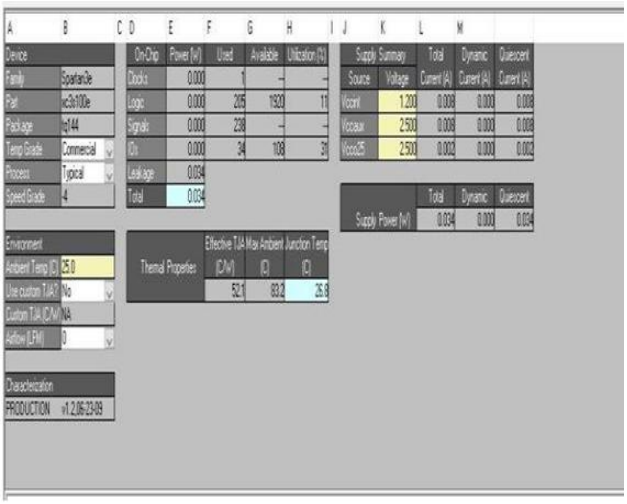

Figure 9: Power Estimation of architecture using ripple carry multiplier and Kogge Stone adder

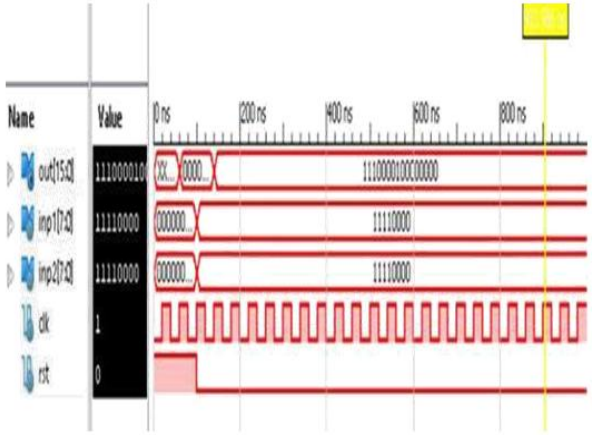

Figure 10: Simulation Waveform of architecture using ripple carry array multiplier and Brent Kung adder

```
Device utilization summary:
---------------------------

Selected Device : 3s100etq144-4

 Number of Slices:                144  out of    960    15%
 Number of Slice Flip Flops:       48  out of   1920     2%
 Number of 4 input LUTs:          262  out of   1920    13%
 Number of IOs:                    34
 Number of bonded IOBs:            34  out of    108    31%
 Number of GCLKs:                   1  out of     24     4%
```

Figure 11: Area of architecture using ripple carry array multiplier and Brent Kung adder

```
Timing Summary:
---------------

Speed Grade: -4

   Minimum period: 7.539ns (Maximum Frequency: 132.644MHz)
   Minimum input arrival time before clock: 27.303ns
   Maximum output required time after clock: 4.496ns
   Maximum combinational path delay: No path found
```

Figure 12: Delay of architecture using ripple carry array multiplier and Brent Kung adder

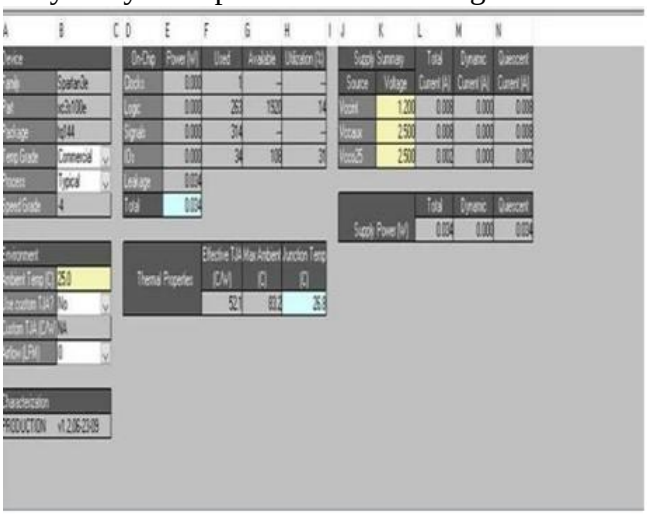

Figure 13: Power Estimation of architecture using ripple carry array multiplier and Brent Kung adder

V. CONCLUSION

This project provides a newly optimized energy detector architecture implementation based on VLSI and such energy detection block can be developed by verilog HDL using XILINX ISE Design suite 14.7 software. Since it has reduced computational and implementation complexity while compared with other alternative techniques. Even though it is simple and popular, the performance is limited than other sensing schemes. In order to improve such performance of energy detection in cognitive radio, the task of performing comparison of energy value with threshold value is important.

As an extension, the existing project can be evaluated by using parallel prefix adder i.e

Ladner Fischner adder in its architecture. We hope to find optimization in both area as well as the timing.

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