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Design of High Performance BIST Based Radix-4 Booth Multiplier Using FPGAs

P. PRASHANTH REDDY[1], P. PRASHATH[2], K. ASHOK BABU[3]

[1]M.Tech in DSCE, Sri Indu College of Engineering & Technology, Sheriguda, Ibrahimpatnam, RR.Dist. HYD

[2]Associate professor, Dept of ECE, Sri Indu College of Engineering, & Technology, Sheriguda, Ibrahimpatnam, RR.Dist. HYD

[3]Professor & HOD Dept of ECE, Sri Indu College of Engineering & Technology, Sheriguda, Ibrahimpatnam, RR.Dist. HYD

Abstract

The ever increasing applications of integrated circuits in the day-to-day useful electronic gadgets are the driving force for the development of low power designs of configurable hardware designs. High speed and low power are the main parameters that are targeted by modern circuit designers. Among the fastest increasing applications the audio and video signal processing applications are growing at a very high rate. Mobile applications have increased the technological improvements for digital signal processing applications. Multipliers are the very important logic operational unit of any processing unit in digital signal processing applications. The speed and performance of multiplier is among the efficiency improvement parameters of any digital hardware design. Another important feature of hardware designs is self-testing ability. This feature provides reliability to the hardware mainly in case of configurable hardware applications. The built-in-selftest (BIST) feature helps in quick diagnosis of the hardware functional authenticity. This paper presents a BIST based implementation of a multiplier. The proposed design is realized using Xilinx Tool (14.7) using Verilog. A low power Test Pattern Generator (TPG) is involved in the design for self-test design realization.

Keywords: Built-In-Self-Test, Test Pattern Generator, Linear Feedback Shift Register, Xilinx.

I. INTRODUCTION

Nowadays, a configurable hardware design performance can be evaluated using its operational speed and power. Field Programmable Gate Array (FPGA) is among the configurable devices that cope with the desired and promising power and speed based hardware performance. In FPGA the operation execution is based on the switching of the internal path of current through a combination of hardware resource architecture. A hardware based optimization of any design can be achieved by the skill based modification of the operational circuit architecture. A low power system offers the benefits like device portability, long battery life, good performance criteria, etc. For modern digital applications a high speed processor with low power requirement design is the basic criteria. The most important design of digital signal processors is the multiplier design. The multiplier is used in most of the complex data processing applications.

The self-testing feature is another feature that is required in the hardware for self diagnosis or self-testing. This feature helps the configurable integrated circuit hardware to test itself and in case of hardware fault it helps to re-locate the hardware resource within the integrated circuit. In the self-test operation, hardware is tested for its functional output with the help of a supplementary hardware. A simple block diagram of a BIST based design representation is shown in Fig 1. Here a Logic Circuit is the design that is a functional block of an integrated circuit hardware design.

In the normal operation mode it performs the defined logic operation on DATA Input. When it is operated in Self-Test mode, a random sequence of data is generated by Test pattern Generator using control signal by BIST Controller. This test sequence is operated by Logic Circuit and the generated output of the logic operation is compared with the actual output. The comparator output indicates logic high if the output of the logic operation against the test inputs does not match with the actual output. This condition indicates a fault in the logic circuit hardware. In such cases a configurable hardware re-locates the circuit resources within the integrated circuit to avoid the faulty hardware.

Many architectural modifications are proposed by many scholars and researchers in their work regarding low power design of BIST based logic circuit for hardware design applications. In [1] a low power test pattern generator design is proposed using a low-power Linear Feedback Shift Register for BIST

Corresponding author: P. PRASHANTH REDDY

structures. This design follows the approach of reducing the switching activity based on single input change pattern generated by a counter and a gray-code converter. Reference [2] presents FPGA Implementation of an LFSR based Pseudorandom Pattern Generator for MEMS Testing. This design has the characteristics of high speed, low power consumption and it is especially suited in the processors where uniform distribution random numbers are required. A Low Power linear feedback shift register based low power test pattern generator design is proposed in [3].

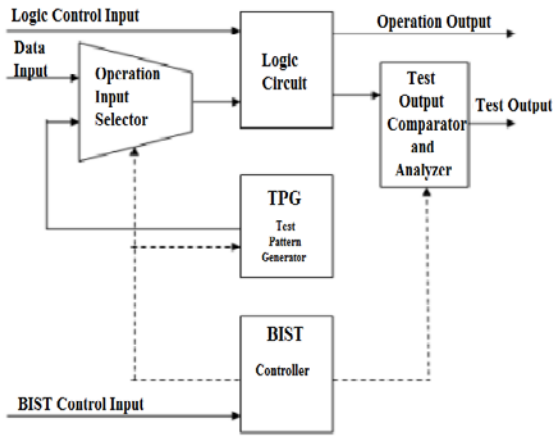


Fig. 1: Simple Block Diagram of BIST Design

This design mainly focuses on how test vectors are generated in the BIST and how to reduce the power consumption. In this paper the transition is reduced by generating the gray-code with 1-bit distance. Reference [4] shows FPGA implementation of 16-bit BBS and LFSR PN Sequence Generator. This paper features the change in the logic of PN sequence generator by changing the seed in LFSR or by changing the key used in BBS. A paper with FPGA based N-bit LFSR to generate random sequence number design is proposed in [5]. This design presents study the performance and analysis of the behavior of randomness in LFSR. A review of LP-TPG using LP-LFSR for Switching Activities is presented in [6]. This paper presents structures of multiplier, LFSR, LP-TPG and BIST. In [7] the author presents a simulation study of TPG using Shift Register based on 16th Degree Primitive Polynomials. The study in this paper focuses on a comparative study of different types of implementations for a LFSR for 16th degree irreducible or primitive polynomials. Generation of Pseudo-Random number by using WELL and Re-seeding method is presented in [8].

In this paper a random number is generated by using WELL method first and its performance was analyzed. For avoiding the repeating pattern the Reseeding method is used. A number of researches are also performed on logic operational units for high speed applications using FPGA devices. A review on Vedic Mathematics for digital signal processing operations is present in [9]. This paper deals with exhaustive review of literature based on Vedic Mathematics. An improved efficiency of Vedic multiplier is proved over conventional multiplier in this paper. An FPGA based implementation of high speed 16-bit Vedic multiplier using LFSR is presented in [10]. This paper describes the implementation of 16-bit Vedic multiplier enhanced with propagation delay and automatic insertion of all possible combinations of inputs. The TPG is the major component of BIST hardware design. Many BIST application circuits are proposed and simulated by researchers to propose power and speed optimized designs based on FPGA implementation. Reference [11] presents FPGA implementation of BIST enabled UART for Real Time Interface Applications. This paper shows functional verification of various block of UART. A concurrent BIST architecture for online input vector monitoring design is proposed in [12]. This paper is based on the idea of monitoring a set of vectors reaching the circuit inputs at the time of normal operation and the use of a SRAM like architecture that store the relative locations of the vectors that reach the circuit inputs. A BIST enabled I2C protocol design implementation on FPGA is presented in [13].

This design enables self-test of a common hardware interface protocol for high speed communication device. The requirement of the today's hardware designs is low power circuit implementation of BIST based logic circuits on FPGA to achieve high speed operational circuits. Reference [14] shows an advanced BIST architecture with Low Power LBIST and BDS oriented March Algorithm for Intra Word Coupling Faults. This paper addresses read faults with classic faults with an improvement in the efficiency of the architecture and test time in detecting the faults. In the present paper a critical consideration is given to low power BIST implementation. A multiplier with two 4-bit inputs is taken as a test design for low power implementation on FPGA with self-test capability. The self-test feature is provided using a low-power test pattern generator design. The test pattern is designed using a modified architecture by reducing the number of sequential component as compared to

the conventional design components. The present paper is organized as follows: Section-II describes the design of Test Pattern Generator and Multiplier that are implemented in this work. Section-III presents simulation and synthesis results. Section-IV presents the conclusion drawn on the basis of the performed design. Finally the references are mentioned.

II. TEST PATTERN GENERATOR AND MULTIPLIER DESIGN

The present work gives the BIST based approach for the implementation of a multiplier using a configurable hardware. A 4-bit low power multiplier design is used as a test logic design in the present work. The multiplier design is implemented using gate level architecture representation for realizing the low-power hardware. The RTL schematic of the multiplier design on Xilinx Synthesis Tool is shown in Fig 2. A gate level combination is used to generate a half-adder and a full-adder design. These adder design block are used in combination to generate the multiplier using the adder terms. For the BIST implementation, a test pattern generator with random output value is required. For TPG realization, a low-power modified design of linear-feedback-shift-register (LFSR) is used in this design implementation. A 3-register is used for the generation of a 4-bit random number. It is a comparative low power design realization as compared to other existing test power generator designs. Most of the existing TPG have a register-to-bit ratio of '1'. In the proposed design, the TPG has a register-to-bit ration of 3:4.

The presented TPG generates a repetitive sequence of four random numbers of 4-bit in sequence as shown in Fig 3. The logic block diagram of the test pattern generator is shown in Fig 4. Three flip-flop with linear feed-back are used. The output of the last flip-flop is XOR-ed with the control input Enable to initiate the random number generation. The outputs of the first two flip-flops are XOR-ed to generate the fourth output bit of the TPG. Thus if Enable input is low then the output of the TPG will drive to logic "0000" output combination. An active high signal on the Enable input will activate the hardware to generate random 4-bit signal. The presented TPG can be used in multiple combinations, serial or parallel or mixed, for generating a random sequence of number with a higher length for many other BIST based application realization. This circuit generates a 4-bit random value using only 3-registers, so relative low power consumption is caused by this circuit. RTL schematic the test pattern generator is shown in Fig 5.

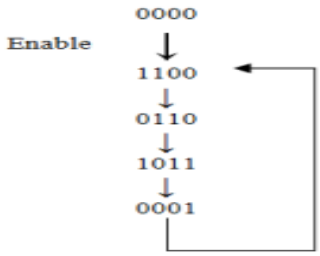


Fig. 2: Flow Diagram of Random Sequence Generation by TPG

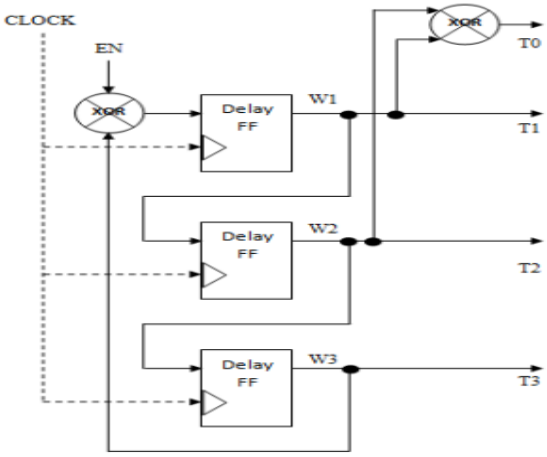


Fig. 3: Logic Diagram of Test Pattern Generator used in Proposed Design

Radix-4 Booth Algorithm

There are various techniques and architectures to perform multiplication in DSPs. The factors differentiating these architectures from one another are delay, throughput, power dissipation, area, complexity of the design. Basic multiplier architectures first compute all the partial products and then use various adders, adder trees to find the sum of the partial products.

Radix-2 array multipliers compute partial products taking into account one bit of the multiplier at a time. Radix-4 Booth multiplier takes into account three bits of the multiplier at a time. This reduces the number of partial products from N to N/2. Let us consider two 4-bit signed numbers X = X3X2X1X0 and Y = Y3Y2Y1Y0 with the MSB indicating the sign (1 for negative and 0 for positive). Three bits of the multiplier X are grouped at a time and encoded [17]. The encoding map is shown in table II. The multiplicand Y is multiplied with P, where P = Xi−1 + Xi − 2 × Xi+1 is the encoded output. −Y is taken as the two's complement of Y , while −2Y is the two's complement of the left shifted Y . 2Y is simply Y shifted one position to the left. The sign extension bits

are the MSB of each row of partial products. The sign extension bits are 0 for positive and 1 for negative partial products. The next row of partial products are then written after shifting it left not once as in the conventional multipliers, but twice as it has four times the weight. The rows of partial products are added to give the final product.

TABLE II: Arithmetic operations to be performed

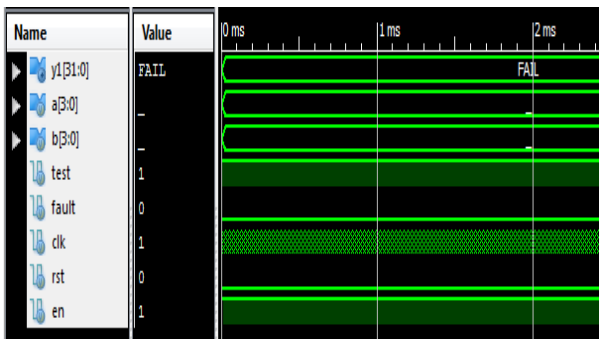
X_{i+1}	X_i	X_{i-1}	$\sum$	A	M	S	Operation
0	0	0	0	0	0	0	No Action
0	0	1	1Y	1	0	0	Add
0	1	0	1Y	1	0	0	Add
0	1	1	2Y	1	1	0	Shift left and Add
1	0	0	-2Y	1	1	1	Shift left and Subtract
1	0	1	-1Y	1	0	1	Subtract
1	1	0	-1Y	1	0	1	Subtract
1	1	1	-0	0	0	1	No Action

Three control signals are generated from P. The first indicating if there should be any action on the multiplicand array (Y) and is denoted by A. A is 0 when there is no action and 1 when there is to be an arithmetic operation. The second decides if the multiplicand array (Y) should be shifted left (2Y is same as shifting Y one time to the left) and it is denoted by M. M is 1 when P is ±2 and 0 otherwise. The third decides whether the multiplicand array should be added to subtracted from the sum and it is denoted by S. S is 0 for addition and 1 for subtraction. The circuit design is proposed in the next section.

III. SIMULATION AND SYNTHESIS RESULTS

The BIST based Multiplier design in the proposed work is implemented using Verilog Hardware Description Language on Xilinx ISE Tool.. The design is simulated for functional performance and power consumption. the simulation wave form is shown in below fig.

Simulation Results:



Synthesize report:

Area:

	Radix-4	**Radix-2**
No. of Slices	81	93
No .of 4 input LUTS	162	180

Power:-

Device	Power (W)
XC3S100e	0.041
XC3S500e	0.088
XC3S1200e	0.166

The power consumption analysis is performed on multiple frequencies and different integrated circuits (FPGAs) with different internal and auxiliary voltage specifications. Xilinx FPGA devices from Spartan3, and Spartan-3E family devices are used for analyzing dynamic power consumption of the present BIST multiplier design. The power-frequency analysis of the proposed work is performed using Xilinx Tool.

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Authors Details:

	**P. PRASHANTH REDDY**[1,] Pursuing M.Tech in DSCE, Sri Indu College of Engineering & Technology, Sheriguda,
	**P. PRASHANTH**[2,] Currently working as Associate professor, Dept of ECE, Sri Indu College of Engineering & Technology, Sheriguda,
	**K. ASHOK BABU**[2,] Currently working as professor & HOD, Dept of ECE, Sri Indu College of Engineering & Technology, Sheriguda