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# Implementation of Dynamic Key Based Stream Cipher using Pipelining in Toeplitz Hash Function

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**Abstract**

Hardware efficient stream ciphers and hash functions are widely utilized in cryptographic applications, for example, data transmission and information security. The onewayness and low hardware complexity of hash function make it a good candidate for authentication operation of crypto-systems. On the other hand, stream ciphers are being widely utilized in the domain of cryptology. Generally, these stream ciphers use static key stream ciphers; the key stream is usually fixed which is either a public key or a private hardware key. However, in this work, we propose a hash function based key generator and integrate the hash function based key generation with the RC4 stream cipher block so as to provide dynamic key to the RC4 stream cipher. Further, this key is utilized to generate the dynamic hardware key for the cryptographic processor. The proposed method is designed for 8-bit hash key and stream cipher utilizing Verilog HDL and simulated using Xilinx ISE 14.7 simulator. Further the design implementation has been done on the commercially available Xilinx Spartan 3E xc3s500e-4fg320 FPGA device. In an effort to extend the speed via pipelining it is proposed to RC4 Encryption and Decryption algorithms.

**Keyword:** Hash Function; Key Generation; Hardware Security; RC4 Stream Cipher; HDL; FPGA

## I. INTRODUCTION

Information technology has become the backbone of modern society, which makes data security an important aspect of research. Now-a-days almost all the confidential facts about the financial status, customers, products, research, customers, or employees, are stored and handled on computers, or transferred to other devices through an accessible physical medium. Information needs to be shared in such a format, which cannot be exploited in a feasible amount of time by any adversary without the knowledge of the key parameters used to encrypt the information. Now-a-days, cryptography has been strongly corroborated in information science using the statistical information theory and number theory [1], [2]. With the emergence of the Internet of Things (IoT) applications, research with focus on robust yet simple crypto-systems have gained importance.

Cryptography can be categorized by the type of encryption operations, the way in which plain text is processed with the numbers of keys used. To secure the data, the encryption algorithm should be fixated to maintain the resistance against the adversary. The updating of encryption and decryption system is necessary as and when the new attack properties are effective. In the security system mechanism of cryptography, the key value ought to be by irreproducible and secret, and it should be challenging for the adversary to decipher the mechanism. Besides the size of key being short, the adversary can interpret the mechanism through brute-force method to retrieve the key value.

In a recent trend, the modern cryptography system utilizes the secure key mechanism of symmetric [3] with asymmetric key cryptography [4] to provide the complete solution to secure the data with authentication. Possessing the trend intact, the paper confesses on the cryptography system which exploits to generate the secured key of symmetric mechanism with the hash function [5]. It provides a virtuous arrangement of performance, efficiency, security, and implements ability. It depends upon the necessity, the researcher may compromise between the security level, throughput and area consumption. The symmetric key encryption plays a vital role, to



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encrypt huge amount of data effectively. However, the symmetric key based cryptography has some solemn issues, namely key management and key distribution [6]. The asymmetric key cryptography [3] was proposed, in order to resolve the key distribution solemn issues in the symmetric key encryption. On the other hand, the family of hash function is an algorithm that maps the data of arbitrary length to the fixed length data. Due to the one-wayness of hash functions, and less hardware complexity, this is the preferred solution to many cryptographic applications [7] where authentication of receiving data is the goal.

In a communication system using RC4 algorithm, the secret master key is shared between the receiver and the transceiver. In this paper, a method of secured encryption and decryption using RC4 algorithm and Toeplitz hash function in the integrated form is proposed where the key is generated using a Toeplitz matrix based hash value generator. This method is designed using Hardware Description Language (HDL) and implemented on the commercially available FPGA device. Further, the randomness test analysis is performed using statistical test methods provided by NIST. The rest of the paper is organized as follows; Section II highlights the cryptographic algorithms such as RC4 and Toeplitz Hash function. The development of proposed model and methodology of dynamic key based RC4 stream cipher along with hash function are presented in section III.

## II. CRYPTOGRAPHY ALGORITHMS

An efficient computational function is the hash function, which maps an indiscriminate length of binary strings of sequence to a fixed length of binary sequences of string called hash value. Hash functions are generally used in cryptography for message authentications [7], the hash values of messages are encrypted and appended to the digital signature as the message, can confirm integrity as well as authentication in the crypto systems. The one-wayness property of the hash function determines the cryptographically strong random number designed based on the hash function. In RC4 stream cipher crypto processor system, key scheduling and random number, generation [8] components are executed to generate the key stream for the encryption and decryption process. The integration of utilizing the hash function for the stream ciphering process is well elucidated in detail here

### A. RC4 Algorithm

RC4 stream cipher [9] is proposed and designed by Ron Rivest for the RSA security of data. The improved and effective version of the RC4 stream cipher is postulated by Jian Xie et al [10] and Weerasinghe [11]. The RC4 stream cipher consists of substitution (S)-box S, an array of length M, every position of S can store one byte of information. To scramble this permutation of all the possible 8-bytes, secret key k of l-bytes size (typically, 5 6 l 6 16) is required. An array L of length M clutches the core key, with the secret key k repeated as L[i] = k[i mod l], for $0 \le i \le M - 1$. In a communication system, the secret master key is shared between the receiver and the transceiver. At the transmitter, encryption is done using simple XOR operation ($C = P \oplus K$) to get the cipher text (C) and the decryption at the receiver side is done using the XOR operation of the cipher text ($P = C \oplus K$) to retrieve the original plain text (P). The Pseudo-Random Generation (PRG) and the Key Scheduling (KS) phases are the main components of RC4 hardware design [2] algorithm is represented in the algorithmic state machine as shown in Figure. 1. Key scheduling phase itself consists of two sub-stages, namely Initialization and Key setup. In the initialization stage, an M-element S −box is generated where M lies in the range from 0 to $2^{n-1}$, where n is the size of the key. The initialized S − box is then permuted based on the provided key L in the key setup stage where a M number of iterations takes place. Then the PRG Phase uses this S−box to generate pseudo random key stream bytes, which are of an arbitrary number. The steps and process of KS, using the Toeplitz hash function and its significance is elucidated in [9], [12].

### B. Toeplitz Hash Function

The hash values are generated by multiplying a message string with random binary matrix. Let E be an x × y matrix with Boolean values, where y and x are message size and hash length in bits respectively. Let Y be a message consisting of y bits and Boolean multiplication of the matrix E by the column matrix of the message Y as the hash value h(E). The matrix is uniquely determined for the first row and column;

the hash function H uses the Toeplitz matrix requires x + y - 1 bits define the whole matrix.

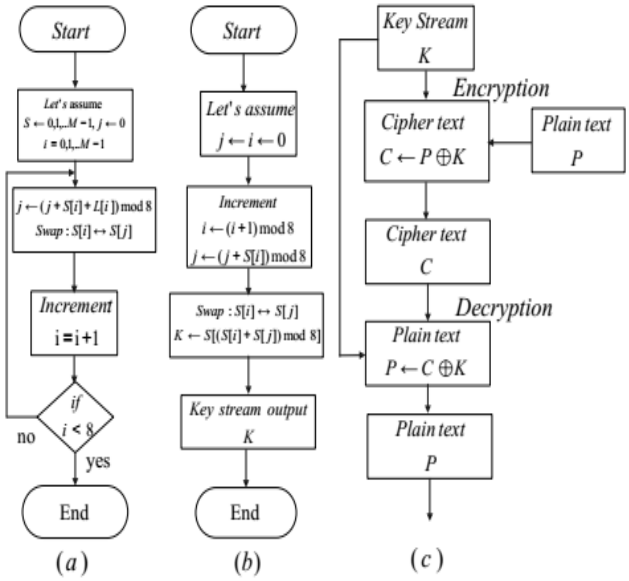


**Figure 1: Algorithmic State Machine to Construct RC4 Stream Cipher: (a) Key Scheduling Phase, (b) Pseudo Random Generation Phase (c) Stream Cipher**

The characteristic property of the Toeplitz matrix is that each value of the column in the binary matrix is achieved by moving down the values of the preceding column and adding the new value element to the first element of the column [15], thus in the Toeplitz matrix each successive element of the column embodies the successive stages of the linear type of feedback shift register. LFSR with the feedback polynomial of degree n, which is used to define the Toeplitz matrix, with the initial seed value of n bits. The hardware architecture for LFSR based Toeplitz matrix for 8-bit hash value is shown in Figure. 2. The constructed LFSR based Toeplitz matrix is Ɛ balanced for $\varepsilon \leq y/2^{x-1}$. The steps to construct the hash value can be well explained as below.

The irreducible polynomial of degree n over GF (2) is represented as g(y), and LFSR generates the sequence of bit a0, a1 - - - with the feedback polynomial g(y) and the initial seed value is represented as a0, a1, - - - , an [16]. Thus for every irreducible polynomial g(y) and initial value of state a ≠ 0, the hash function is associated with the message Y consisting of y bits of binary length as the linear function of the combination.

Let's consider the irreducible feedback polynomial for generating the hash value using the LFSR polynomial g(y) = x 8 + x 4 + x 3 + x 2 + 1 and the initial value of LFSR is considered as (a0, a1, - - -, a7) = (0 1 0 1 0 0 1 0). To determine the requirement of the hash function in the Toeplitz matrix, should satisfy x + y - 1 bit, the output sequence from LFSR should produce only 9-bits where x is the degree of g(y) is 8 and the message bits y = 8 (thus, 8 + 8 - 1 = 15 bits). With the above irreducible polynomial g(y) of degree 8 and with the initial seed value, the 15 bit sequence LFSR output is (a0, a1, a2, · · · , a14) = (0 1 0 1 0 0 1 0 1 0 0 0 1 0 0). Toeplitz matrix is formed by starting the initial value of LFSR,

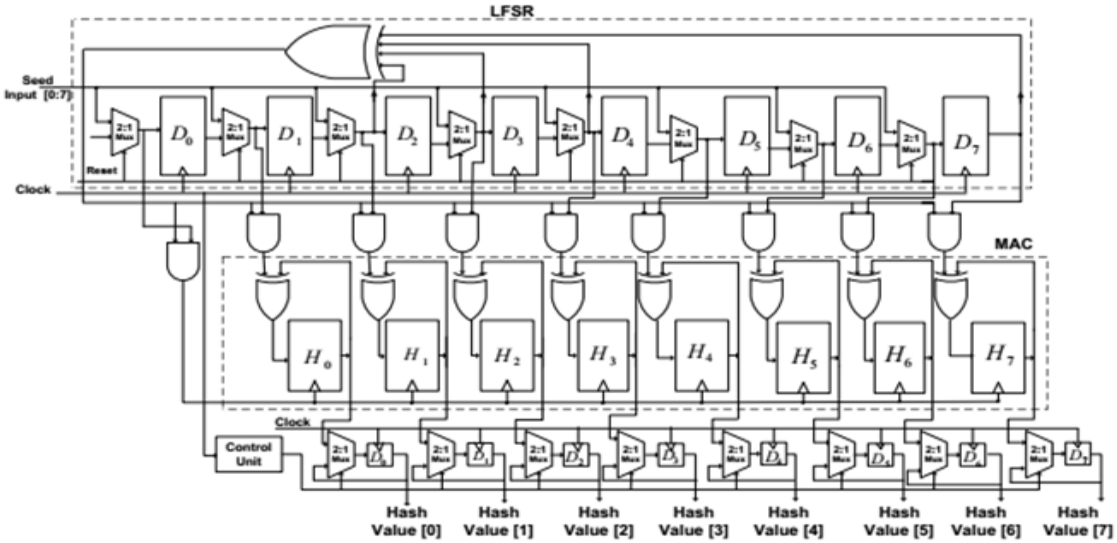


**Figure 2: 8-bit Hardware architecture and Implementation of LFSR based Toeplitz hash function**

LFSR Output Sequence =[0 1 0 1 0 0 1 0 1 0 0 0 1 0 0]

Toeplitz matrix (8 x 8) =

$$\begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 \end{bmatrix}$$

for each values of the column in the binary matrix is achieved by moving down the values of the preceding column and adding the new value element to the first element of the column, thus in the Toeplitz matrix each successive element of the column embodies the successive stages of the linear type of feedback shift register is achieved after every clock cycle to top of the each column.

Let's assume the message bits be [1 1 0 0 1 1 1 1], thus multiplying the message in column matrix with the Toeplitz matrix which is obtained with the LFSR output Sequence determines the Toeplitz matrix of (8 x 8) is given above and the hash value output is [0 1 1 0 1 0 0 0]$^T$ . The hash value for the corresponding message bit can be a secret key to RC4 as discussed.

$$\begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \end{bmatrix}$$

$$= [0\ 1\ 1\ 0\ 1\ 0\ 0\ 0]^T$$

## III. EXISTING METHODOLOGY

The proposed model and method consist of the Toeplitz matrix based hash function, which provides hash value as a key to the RC4 stream cipher is shown in Figure. 3.

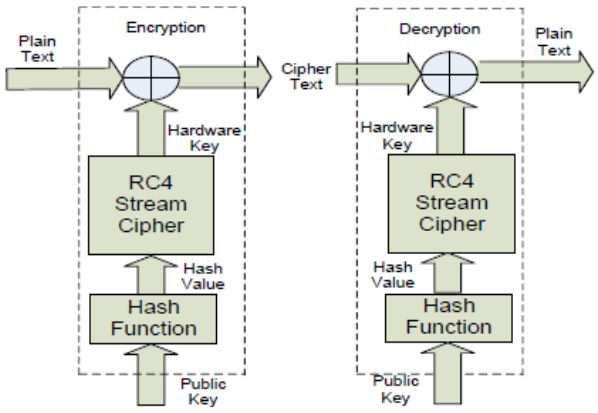


**Figure 3: Methodology for Encryption and Decryption**

The output key stream of the stream cipher is used to encrypt the plain text message using the XOR operation. The Toeplitz matrix based hash function requires the message which is to be encrypted, is used to generate the hash value. In this method, the public key (message) which will be shared between the encryption and decryption process. A continuous stream of message is fed as input to the hash function block to generate the stream of the hash value. This operation is processed using the public key which is saved in the register memory bank and it is fed to generate the hash value by right shifting the operator bit by bit [17].

LFSR based PRNG's output bits are multiplied with the input bits, which can be achieved using AND gate and passed on to the MAC (multiply-and-accumulate) unit (using AND-OR logic) so as to accumulate it over a specified period of time (n clock cycles). The output is pushed every n th clock cycle using a multiplexer which is controlled by a control unit. The control unit consists of a conventional counter and it produces a transition signal after every y clock cycle, where y is the size of the message to be hashed. This output is then provided as key (L) to the stream cipher block.

In a conventional RC4 stream cipher, the key stream is usually fixed which is either a public key or a private hardware key [18]. However, in this proposed design, we have constructed the dynamic key stream where the key k stream is replenished on every n cycle by a hash value of the public key as shown in the Figure. 4, schematic structure of proposed design. We have used an LFSR based Toeplitz matrix is used to generate the hash value. In general, a fixed x × y Toeplitz matrix is used to generate the hash value where the LFSR is reset after every computation of the hash value. But since the input to the hash value generator is the public key k in every cycle, this method would generate the same hash value every time.

In this methodology, the hash value itself changes over time since the LFSR based Toeplitz matrix is not reset except for a global reset. Thus the Toeplitz matrix only repeats after the total number of 2 n cycles, where n is the number of bits of the LFSR. The motivation of having a dynamic key for the RC4 algorithm is to increase the security of the whole crypto system. Moreover, since hash function is one-way, it is considerably infeasible to get the public key

even if a cryptanalytic attacker is able to find a particular key k. Thus, it will again be very difficult to trace the next key stream value which is generated from the hash function. Initially, the crypto system waits for the n cycles to get the hash value generated. Once the hash value is ready, the RC4 algorithm is initiated to generate the key stream. After the first n clock cycles the hash function and RC4 algorithm operate in parallel. Henceforth, for every n clock cycle a new hash value is generated and replaces the value of the Key (L), thus realizing the dynamic key for the RC4 stream cipher.

## IV.PROPOSED METHODOLOGY

The proposed model and method consists of the Toeplitz matrix based hash function using pipelining which provides hash value with high speed used as a key to RC4 stream cipher is shown in Figure 4.

A common technique for increasing the throughput of electronic circuits is that of pipelining. Pipelining consists of breaking long combinatorial paths by introducing clocked memories; this has the effect of dividing the circuit into sections, in which calculations are run independently. The output of a pipeline section becomes the input of the next one at each clock cycle; while generally preserving the global latency, pipelining increases the throughput of a circuit because several instances of the problem are injected at each clock cycle and are processed independently inside each of the sections. The clock pulse is reduced as a result of the breaking of the combinatorial path, thus allowing higher clock frequencies to be used.

At the initial stage of the process in LFSR, the seed value is loaded into registers, using a clock. The seed input values are then loaded into the flip-flops and to the corresponding output, once the input value is high. The previous state output is XORed with the current state value and it is stored as the present state value, during the active low input state. LFSR based PRNG's output bits are passed into registers where pipelining operation is done. The output bits are multiplied with the input bits, which can be achieved using AND gate and passed on to the MAC (multiply-and-accumulate) unit (using AND-OR logic) so as to accumulate it over a specified period of time (n clock cycles). This output is now passed through registers where pipelining operation is done to decrease the delay. The output is pushed every $n^{th}$ clock cycle using a multiplexer which is controlled by a control unit. The control unit consists of a conventional counter and it produces a transition signal after every y clock cycle, where y is the size of the message to be hashed. This output is then provided as key (L) to the stream cipher block.

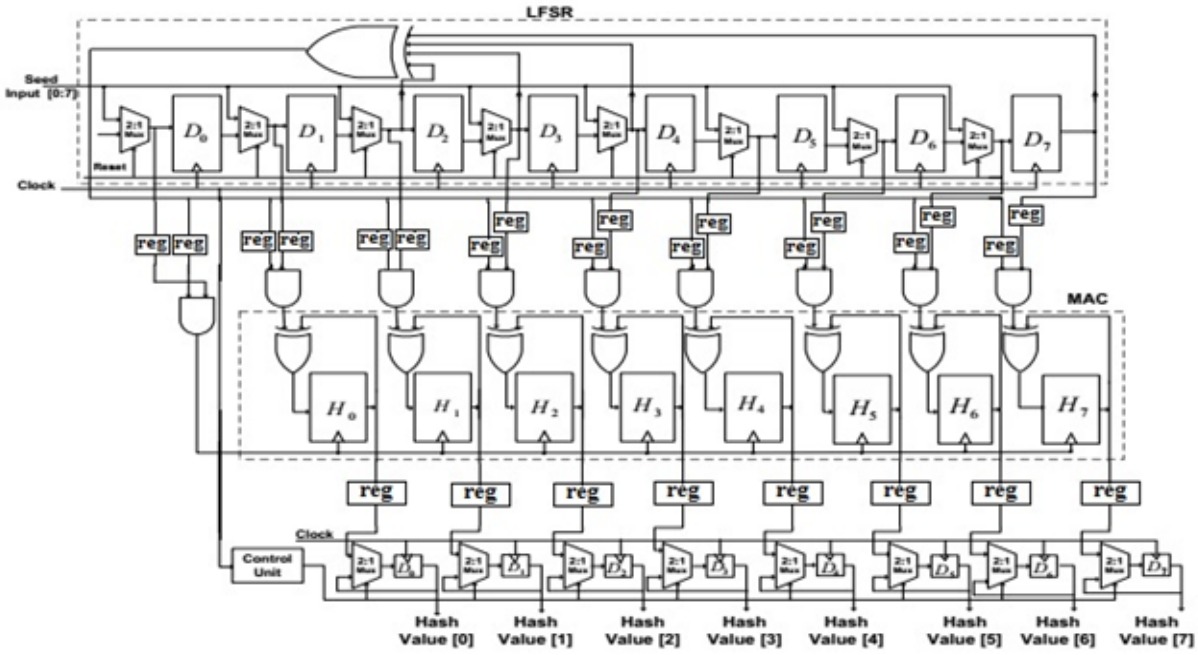


**Figure 4: 8-bit Hardware architecture and Implementation of LFSR based Toeplitz hash function using pipelining**

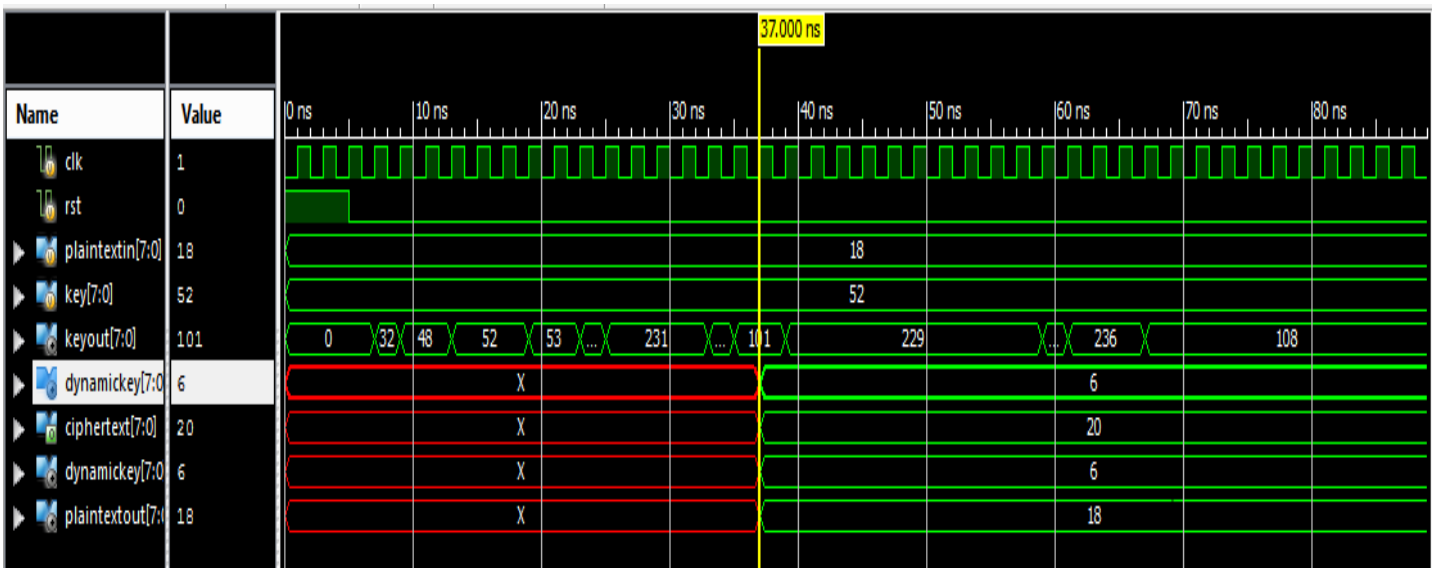


**Figure 5: HDL simulation Result of Proposed Design**

## V. SIMULATION RESULTS

The proposed method is simulated and synthesized using VERILOG HDL on Xilinx 14.7.The simulation result of generating a hash value for the corresponding message bit using pipelining is shown in the figure .5 are further used to construct the random dynamic key from the 8-bit seed. The synthesized report for logic utilization is summarized in Table I. The proposed integrated design of generating hash values using pipelining is implemented on Xilinx 14.7. The device utilization of the implemented design and proposed design are shown in Table I and Table II respectively.

**Table I**

| Logic Utiliztion | Used |
|---|---|
| Number of slice | 19 |
| Number of slice Flip Flops | 24 |
| Number of 4 input LUTs | 34 |
| Number of bonded IOBs | 18 |
| Number of GCLKs | 1 |

**Table II**

| Logic Utilization | Used |
|---|---|
| Number of slice | 33 |
| Number of slice flip flops | 55 |
| Number of 4 input LUTs | 35 |
| Number of bonded IOBs | 18 |
| Number of GCLKS | 1 |

The existing design and the proposed design is also implemented on the same Xilinx 14.7 for the fair comparsion. Thus, the implementation of the Toeplitz hash function in reference to delay, power and figure of merit is presented in Table III.

**Table III**

| | Delay | Power | Figure of merit |
|---|---|---|---|
| **Toeplitz Hash Function** | 4.507ns | 88mW | 396.616 |
| **Toeplitz Hash Function with Pipelining** | 3.872ns | 87mW | 336.884 |

## VI. CONCLUSION

In this paper, a new design is proposed for optimization of Toeplitz hash function using pipelining. The method is particularly indicated to enhance the speed the circuit, is of easy and direct formulation, and can be used to effectively to generate hash values. The proposed design is simulated and synthesized by using Xilinx 14.7.The comparison result shows that the proposed design with less delay, power and figure of merit can be good candidate and suitable for hardware cryptographic applications.

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