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AN EFFICIENT AND HIGH PERFORMANCE SOVA DETECTOR ON FPGA

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Abstract

Soft output Viterbi detectors (SOVA) are generally used in all communication receivers within the digital back-end circuitry for explanatory inter symbol interference. Present implementations of the SOVA detector are based on uniform quantization using register exchange logic or with a trace back approach. In this paper, we examine the design architecture and performance examination of a SOVA detector based on non-uniform quantization. The proposed detector was synthesized and place and routed using Xilinx tool chain and implemented on Spartan -3E XC3S1200E-4FG320 field programmable gate array (FPGA) kit. Execution results in FPGA shows that our projected architecture results in decrease in the total number of slice registers decrease in the number of slice look-up table (LUT) and reduction in the delay.

Keywords: SOVA, sliding block, high-throughput, nonuniform quantization.

I. INTRODUCTION

Coded communication over a channel, such as read channel in a magnetic recording systems, requires a soft input soft output (SISO) detector to contest the inter symbol interference (ISI) [1]. The detector is naturally attached to an error correction decoder within a turbo equalization setup [2] to improve the information bits from the equalized samples, post analog front end. Though the maximum a posteriori (MAP) algorithm [3] is an optimum detection algorithm in terms of symbol or bit error probability, it has not been a popular choice from very-large-scale integration (VLSI) design architecture side due to implementation difficulty. The SOVA [4], which is a alteration of the unique Viterbi algorithm [5] approximates the max-log MAP algorithm with a much minor computational complexity and is the favored choice for the plan of soft output detectors. With technological progress, there is a need for the efficient design of high speed detectors with reduced area and power consumption keeping up with increasing data rates, storage and other communication systems.

Various architectures for high throughput implementation of SOVA have been proposed in the literature. The primary high speed design was projected by Joeressen and Meyr . Their circuit achieves a throughput of 40 Mbps with a two step SOVA with trace back approach. A decoding rate of 100 Mbps was achieved with a bi-directional SOVA algorithm. In terms of power consumption, this method is inefficient, as it performs the exact same calculations twice. In another approach, a high decoding rate was achieved by replacing a radix-2 trellis by a radix-4 trellis. This method results in a 2x speedup at the cost of computational and hardware complexities by the same factor. A systolic array processor, with path metrics and decision vector propagating in register pipeline, achieve high throughput at the cost of massive register count and power consumption. Both the disadvantages were alleviated by replacing the register pipeline with an orthogonal memory by the work in. Nonetheless, the usage of a transistor level advanced orthogonal memory is impractical in FPGA for compositional investigation. A 500 Mbps SOVA decoder was composed in by changing the include look at select (ACS) recursion to perform include and contrast operations in parallel driving with an expanded throughput. Further, the requesting of include, look at and select operations in the ACS unit is adjusted to decrease the basic way in the outline.

This is the most extreme achievable throughput revealed in the writing utilizing a solitary SOVA indicator/decoder. Here every implementations of SOVA, a trace back approach is adopted. This essentially comes with high latency and storage necessities. To achieve high throughput beyond 2 Gbps, a fully unrolled pipelined architecture is

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needed. The recursive character of the ACS unit prevents the pipelined implementation of the detector. The above limitation was removed in by using a sliding block Viterbi decoding/detecting (SBVD) approach. The sliding block approach allows block-by-block detection of a continuous stream of data bits in an area efficient manner. Block independence is achieved by forming the overlapping blocks out of the incoming data stream individually processed by the Viterbi algorithm.

The quantization of a choice of internal parameters of the detector has a straight impact on the VLSI path In this document, we suggest a novel non-uniform quantization of the likelihood values of the SOVA detector, motivated from the non-uniform quantization of low-density parity check (LDPC) codes in, to reduce the overall area of the detector footprint, while achieving the same signal to-noise ratio (SNR) performance as uniform quantization. We introduce two non-uniform quantization designs for the detector.

Relative focal points of both the plans have been contrasted and the ordinary uniform quantization. Whatever is left of paper is composed as takes after. In Section II, we give a concise depiction of the SOVA calculation took after by an itemized talk of the execution examination and a strategy to deliberately decide the outline parameters utilizing non-uniform quantization. In Section III, we portray the plan design of the proposed finder took after by the depiction of the test setup and the execution comes about because of FPGA in Section IV. At long last, we close the paper in Section V.

II. SOVA ALGORITHAM

The read direct in attractive capacity gadgets post simple front end, comprises of a limited motivation reaction (FIR) straight versatile equalizer, trailed by a SOVA indicator. The previous evens out the channel, with the end goal that it coordinates a fractional reaction (PR) target [1]. The PR focus of request N, can be spoken to by a trellis, with 2N states. The Viterbi calculation finds the in all probability (ML) arrangement utilizing the trellis outline. Each info grouping compares to a known way in the trellis. The indicator appoints to each branch, a branch metric which is figured as the square of the Euclidean separation between the got image and the yield image relating to that stem. To each state in the trellis, a state metric is relegated. This metric is a measure of possibility of that state. It is computed as the base of the amassed way measurements coming to that state. Once the finish of the trellis is achieved, the way with the base way metric is announced as the ML way. The comparing bit esteems related with that way are announced as the identified piece arrangement. SOVA goes one stage forward in computing the dependability of the recognized bits by monitoring the contending ways along the ML way. To delineate the above point, proceeding with Hagenauer's documentation [4], let M1 and M2 signifies the two ways measurements of the two ways converging to the state s. Further, accept that way 1 is the ML way as identified by the Viterbi calculation (i.e., M1 ≤ M2). As recommended in [4], the log-probability proportion (LLR) for bits in every one of the positions where the two contending ways contrast is given as:

$$L_j' \leftarrow \min (L_j, \Delta), \qquad (1)$$

where, Lj means the already put away LLR esteem for the jth bit, **Δ** = M2 − M1 indicates the way metric distinction between the contending ways converging to the state s and L J signifies the new refreshed LLR esteem for the jth bit. This refresh must be done for every one of the bits along the ML way where the bit choices between the ML way and the contending ways oppose this idea. The sliding piece approach proposed in for hard yield Viterbi unraveling is stretched out in this paper to create delicate unwavering quality estimations of the recognized bits. This approach permits a high throughput configuration by permitting autonomous location in a range proficient Manner.

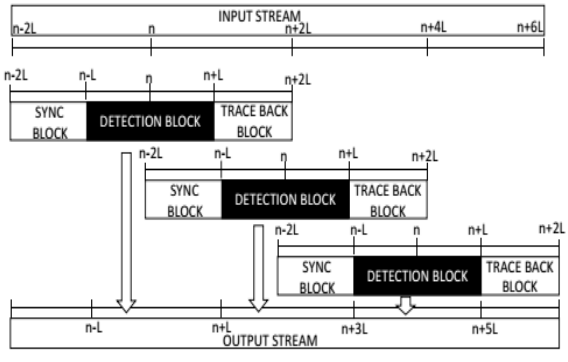

Figure 1: Block processing of continuous stream of data using sliding block viterbi detector. The length of each block is L while the length of the detection depth is 2L.

With a specific end goal to distinguish bits in the scope of n − L to n + L, data from n − L − K to n + L + M is required as appeared in Fig. 1, where K is the synchronization length and M is known as the survivor way length of the finder. We have picked K = M = L for straightforwardness. Here, the scope of qualities from n−L to n+L is named as the discovery profundity (dd) of the indicator. This likewise speaks to the delicate refresh window i.e., the unwavering quality estimations of the bits existing in this window are just refreshed. The aggregate square length from n−2L to n+2L is known as the window length (w) of the identifier. Since there is no systematic recipe for count of parameters like w and dd of the locator, these were resolved through recreations. Fig.1 demonstrates that w = 16 and dd = 8 is an ideal decision as the bit blunder execution indicates just a debasement of 0.3 dB at a bit mistake rate (BER) of 10−4 contrasted with a state introduced Viterbi locator. A state instated finder is a square handling indicator in which each piece gets state introduced from it's past piece. It is seen from Fig.2. that for a settled proportion of w to dd, bigger esteems for w gives enhanced execution, as it considers bigger number of tests for identifying the bits. Further, for a given w, bigger dd prompts poor piece blunder rate. The purpose behind this is littler dd for a given w implies bigger estimation of synchronization length and follow back length, which would in the long run prompt an enhanced execution of the indicator. It is to be noticed that for a given w, a bigger dd is favored as it would in the end prompt bigger throughput of the locator. A littler w would prompt a decreased region overhead of the identifier, whereas, bigger w are normally favored for bring down BER and enhanced throughput in light of the fact that bigger w will prompt a bigger incentive for identification profundity for the same BER execution. In this way, the decision of w and dd is an improvement issue between throughput, range and execution. To assess the nature of the delicate yield delivered by the SOVA identifier, a linked framework is shaped comprising of the SOVA finder took after by a LDPC decoder of code length 4096 and code rate 3/7. Fig. 3 demonstrates the execution plot for such a framework. It is seen from the assume that the SOVA identifier - LDPC decoder framework demonstrates an execution pick up of 4 dB contrasted with a framework shaped by hard Viterbi indicator took after by a LDPC decoder at a BER of 10-4.

QUANTIZATION:

The decision of quantization significantly affects the territory and power utilization of the last plan. We present a novel non-uniform quantization conspires where the quantization step measure changes with the information greatness. Contributions with littler greatness are quantized with littler stride measure. With expanding greatness, the progression estimate is likewise expanded, prompting a bigger dynamic range contrasted with uniform partner. We propose two plan structures utilizing NUQ. In the main plan, NUQ is performed for all the inner parameters of the finder like the branch metric, state metric and the probability esteems, while, in the second outline, just the probability esteems put away in the delicate era unit of the locator are non-consistently quantized. The non-consistently quantized execution plot comparing to the principal configuration is named as NUQ-1, and the execution plot relating to the second plan is marked as NUQ-2 in Fig. 2 and Fig. 3 These figures demonstrate that with practically an indistinguishable BER execution from uniform quantization, NUQ-2 lessens the limited word length of the probability esteem by a bit, while, NUQ-1 accomplishes a similar execution with each of the quantization parameters diminished by one piece. The motivation behind why with a similar word length NUQ gives preferred execution over uniform partner can be followed to the expanded dynamic range in NUQ. We will indicate later in area IV-A that from usage point of view NUQ − 2 is superior to both uniform quantization and NUQ − 1. To delineate the proposed non-uniform quantization conspires; consider a uniform quantization plot with q bits. Give us a chance to accept that we are managing positive numbers as it were. Subsequently, with uniform quantization, the dynamic range and step measure are 0 to 2q − 1 and 1 individually. Non uniform quantization conspire accomplishes a similar dynamic range with just q − 1 bits with fluctuating quantization step estimate as showed in Table I for q = 4. The variety of step estimate (s) with the information (x) is given as:

$$S=n \text{ for } \sum i=0^{\wedge} n-1 \; I \; 2q-(i+1) \leq X \leq \sum i=0n \; i2q-(i+1) \quad (2)$$

Where, n = 1, 2, 3, ...n.

DESIGN ARCHITECTURE:

High Level description:

In every one of the executions of the SOVA detailed in the writing, a two-stage process is embraced. In the initial step, hard Viterbi calculation is connected to discover the ML way in the trellis. Once the ML way is resolved, trace back is completed along the ML way by refreshing the unwavering quality estimations of the bits to be recognized by (1). In this paper, we propose a solitary stride sliding piece SOVA indicator, the square schematic of which is appeared in Fig 5. Here, both the hard yield and the delicate unwavering quality esteems are produced in an enlist trade way, dispensing with the trace back procedure totally.

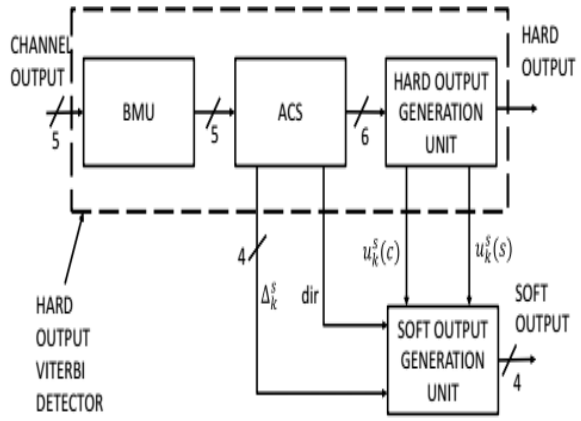

Figure 2: Block diagram of the sliding block SOVA detector

LOGIC DESIGN:

Branch metric unit (BMU):

The BMU ascertains the branch metric for each change in the trellis at time n as the square of the Euclidean separation between the identifier contribution at time n and the yield image comparing to that progress branch. Fig. 3 gives the inner design of a 3 bit BMU. It initially computes the modulus of the contrast between the finder input and the yield relating to a trellis branch. The distinction esteem is then sustained as deliver bits to a look-into table (LUT) that stores the non-uniform or uniform quantized variant of the square of these distinction esteems.

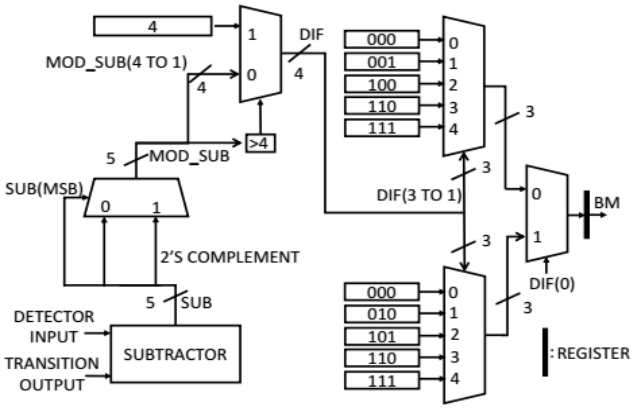

Figure 3: Block diagram of branch metric unit

The modulus of the difference between the detector input and output corresponding to the branch is stored in the DIF. Square of this difference is calculated by referencing through a non-uniformly quantized LUT.

Add compare select unit (ACS):

As indicated in Fig. 4, the ACS unit finds the cumulative path metric arriving to a particular state by adding state metric of its predecessor states to the branch metric on the transition from the predecessor to that state. In case of NUQ state metric, the adder block in Fig .4 is replaced by a LUT holding non-uniformly quantized version of the sum. In another implementation of NUQ (adopted in NUQ-1), the uniform adder is used to perform the addition operation. But, the state metrics are stored as non-uniformly quantized values. This reduces the word length for storage by a bit. But, it requires additional conversion circuits from uniform to non-uniform conversion and vice-versa.

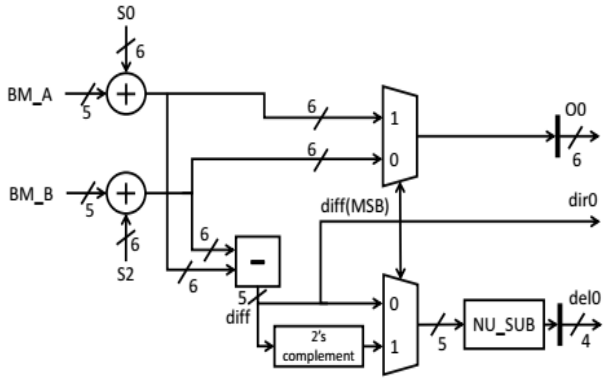

Figure 4: Piece outline of ACS.

BM An and BM B speaks to the branch metric of the two branches converging to the state 0 from the

forerunner states with state metric S0 and S2, separately. NU SUB is the uniform to non-uniform transformation piece. dir0 speaks to the survivor way data for state 0. The distinction in the way measurements of the two contender ways converging to state 0 is put away as del0.

Since we are worried about double trellises, there are two ways converging to a state. The littler of the two aggregate way measurements touching base to a state is chosen as the state metric for the present state utilizing a comparator multiplexer blend. The total estimation of distinction in the two way measurements is gone through a uniform to nonuniform converter circuit (alluded as NU SUB in Fig. 4 acknowledged utilizing LUT. The non-consistently quantized esteems are utilized for unwavering quality refresh in the delicate yield era unit.

Hard output generation unit:

Using a two dimensional exhibit of registers that are interconnected as a trellis, hard yields are created utilizing the enroll trade technique. In this strategy, each state is related with an enlist that records the identified piece succession along the way from the underlying state to that state. This technique has a low dormancy and is especially reasonable for high throughput outlines.

Soft output generation unit:

The soft generation unit unit is utilized to decide the unwavering quality esteems related with the distinguished bits utilizing register trade technique. The LLR refresh for somewhat relating to a state ought to be done, if the bit an incentive for the two contending ways to the state differ and the distinction in way measurements of the two ways is littler than the already put away unwavering quality incentive for that bit.

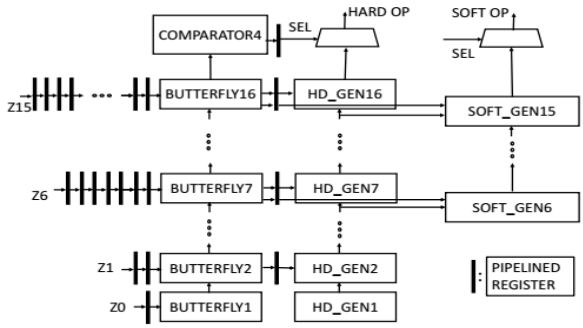

Figure 5: Detailed design of SOVA detector

The BMU and the ACS unit are pipelined using two pipeline registers to form the butterfly block which can be replicated along with the hard output and soft output invention blocks to understand a completely pipelined version of the sliding block SOVA detector to achieve very high throughput. Fig: 5 shows the general architecture of the proposed detector.

Simulation and Synthesize Results:-

Simulation wave forms:

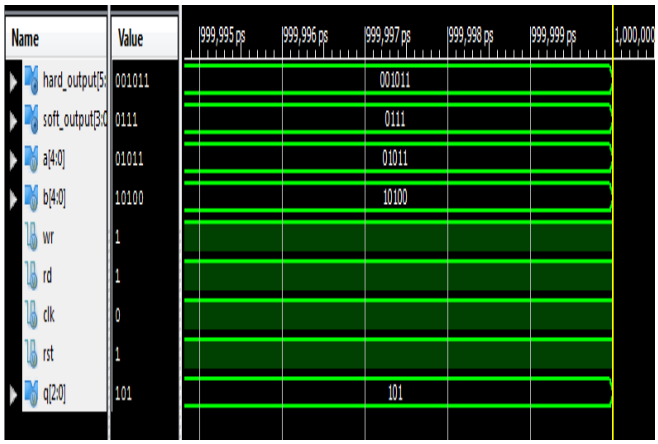

Figure 6:

Synthesize report:

Area:

Table 1:

	Existing	Extension
No of Slices	**246**	**192**
No of 4 input LUT's	**364**	**359**

Delay:

Table 2:

	Existing	Extension
Delay	**6.713 ns**	**5.978 ns**

V. CONCLUSION

In this Project we designed a novel non-uniformly quantized high- throughput soft-output Viterbi detector based on sliding block architecture for an FPGA circuit prototype. When compare to existing method the proposed method is efficient in area and The proposed detector was synthesized and place and routed using Xilinx tool chain and implemented on Spartan -3E XC3S1200E-4FG320 field programmable gate array (FPGA) kit.

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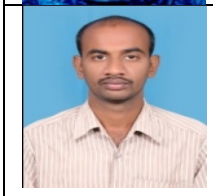	**G.Ravi Kumar,** is an Assistant Professor at Vidya Jyoti Institute of Technology, Aziz Nagar, Hyderabad. He received his Bachelor degree in Electronics and communication Engineering and pursued M.Tech in VLSI System design from JNTUH affiliated college.