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Design of High Performance and Efficient Blowfish Algorithm by using 512 ROM Based S-Box

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Abstract

It is well-known that advanced encryption standard (AES) algorithm is used for protection against various classes of wireless attacks in wireless communication standard such as Wi-Fi, Wi-MAX, Zig-bee and Bluetooth. However, the AES is a complex algorithm that consumes a larger design core, time, and power source. Hence, this paper presents a development of an improved power-throughput Blowfish algorithm on Zynq-7000 field-programmable gate array (FPGA) as an alternative security algorithm. The proposed memory-based method is used to optimize the performance of Blowfish. The performance is analyzed in terms of its architecture, throughput, and power consumption. Results show that the proposed Blowfish reduces slice usage by 63% and increases throughput by 29% at low power consumption.

Index Terms: advanced encryption standard, Blowfish, security, power-throughput, field-programmable gate array.

I. Introduction

Currently, security has become a serious concerned in wireless communication standard. Research trends also more focused on small high-speed security architectures and systems with low power consumption for mobile devices because they are compact and have limited battery power. By referring to a study investigated by [1-7] on the performance comparison between advanced encryption standard (AES) and Blowfish, the result shows that the AES actually consumes more power and time than Blowfish. Blowfish was designed in 1993 by Bruce Schneider as a free and simple alternative to existing security algorithms. Blowfish has a 64-bit block size and a variable key length from 32 bits to 448 bits [8]. The Blowfish algorithm consists of two units: key expansion and data encryption units. Figure 1 shows that the 64-bit text input is divided into two 32-bit halves in this algorithm. Blowfish uses P-array (P1-P18), which consists of 18 32-bit sub keys for key expansion unit, and has 16 rounds, with each round implementing the Feistal (F) function. In the F function block, four 32-bit S-boxes have 256 entries each. After the 16th round, two 32-bit halves data are recombined to obtain the cipher text.

This paper proposes a development of improved power throughput Blowfish algorithm on a Zynq-7000 xc7z020 field programmable gate array (FPGA) platform. FPGA is used for the implementation process because it can be reconfigured for multiple tasks with only a single chip. The Zynq-7000 family offers the flexibility and scalability of an FPGA, while providing performance, power, and ease of use typically associated with application-specific integrated circuit (ASIC) and application-specific standard parts (ASSPs). The range of devices in the Zynq-7000 all programmable system-on-chip (SoC) family allows designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools.

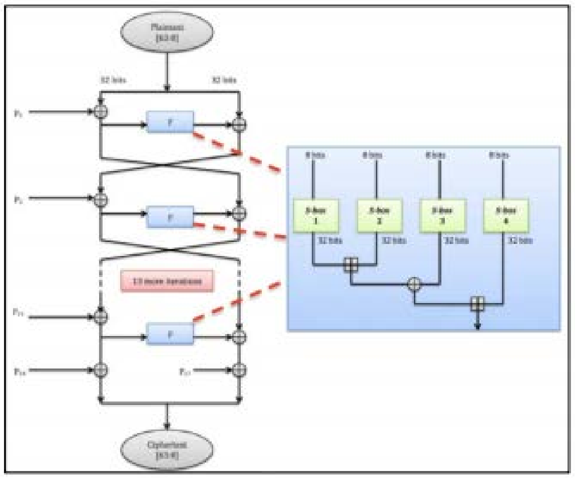


Figure 1: Blowfish Algorithm with F Function

The proposed Blowfish is designed using a memory-based method to improve its performance. This design is extensively evaluated based on three areas. The first area is the architectural parameter, which is used to obtain a minimum hardware requirement that can lead to a smaller design size. The second area is a high-throughput design to carry out an encryption/decryption as fast as possible. Finally, the third area is the low power design, which seeks to minimize power consumption at all costs. This comparison can help researchers decide on the possibility of implementing Blowfish for a secure wireless communication instead of AES.

This paper is organized as follows. Section 2 discusses the related works on Blowfish designs. Section 3 introduces the improved power-throughput Blowfish architecture. Section 4 analyzes the performance of the proposed Blowfish in terms of architecture, throughput, and power consumption. Finally, Section 5 presents the conclusion.

II. Related Works

This section discusses the related studies on Blowfish designs. These works are presented to show the performance comparison in terms of architecture, throughput, and power consumption using FPGA. Not all studies on the Blowfish algorithm were designed with very high-speed integrated circuit hardware description language (VHDL) or Verilog, whereby the design can be simulated and then implemented on FPGA for verification. Most studies analyzed performance based on simulation by only using Matlab, CPU processor, and schematic, which will not be discussed in this section.

A soft-core implementation of the Blowfish cryptographic algorithm known as SCOB, was proposed by Salomao et al. [9]. This soft-core processor is oriented toward applications that demand a high throughput and exploit both the spatial and temporal parallelism available in the Blowfish algorithm [9]. A VHDL was used to design this Blowfish and implemented on Altera Flex19K epf10k250agc599-1 FPGA. The design utilizes six random access memory (RAM) and was run at 10 MHz of clock frequency. Singpeil et al. [10] proposed an implementation of the Blowfish algorithm in the commercial FPGA coprocessor micro Enable to obtain a high performance design. The speed of Blowfish computation was increased by a factor of 10. The operating frequency for this Blowfish was 10 MHz

A VHDL model of Blowfish was designed by Raghuram et al. [11]. its architecture consists of addition, subtraction, modular multiplication, exponentiation, and XOR units. A high data rate is achieved by applying loop unrolling to the Montgomery algorithm [11]. The maximum clock frequency of this design is 77 MHz Sudarshan et al. [12] proposed an architecture using dynamic reconfiguration, replication, inner loop pipelining, and loop folding techniques. It was implemented on Virtex2 2v500fg456-6 FPGA with a clock frequency of 146.515 MHz another Blowfish algorithm was developed and implemented on Virtex xcv50bg256-6 FPGA by Karthigai Kumar and Baskaran [13]. The iterative method was used in their work to reduce the occupied area. Only a single register was required instead of a huge number of registers, which gives feedback to itself for each round. Thus, four memory ports for four S-boxes and one memory port for Parray are needed for their design. The Blowfish design was run with a clock frequency of 95 MHz.

Dakate and Dubey [14] designed a Blowfish with a 128-bit key size using VHDL, and it was implemented on Altera Quartus II FPGA. The key generation of using the F function was proposed. However, their study did not discuss the clock frequency and design size of their Blowfish algorithm. The latest Blowfish design on FPGA was presented by Chatterjee et al. [15]. The algorithm was developed using Verilog and verified through Spartan3E xc3s500e-5fg320. They used a pipelined approach to design the algorithm to improve its throughput. Their architecture showed that the data path of sixteen module blocks is measured by a control unit. Their Blowfish design was operated at 295.63 MHz with a latency of 49 clock cycles.

III. Proposed

Blowfish In this study, an improved power-throughput Blowfish algorithm was designed using Verilog. The architecture of the proposed Blowfish consists of a 128-bit block size and key size, whereby it comprises two parallel blocks of 64-bit Blowfish algorithm that are simultaneously executed. This design technique enables the throughput of the Blowfish algorithm to be maximized. As shown in Fig. 2, the parallel blocks share the same S-box that is used for the F function. On Spartan 3E FPGA, BRAM is utilized to store the four 32-bit S-boxes where the performance can be improved by decreasing the delay into the clock-to-out value of the flip-flop (FF) [16]. The mode is used to select for encryption or decryption.

As the implementation of the Blowfish design is targeted to reduce the core size and timing delay, the proposed memory based S-box method is optimized as illustrated in Fig. 3(a). Based on the Verilog design module, In the existing method uses a read-only memory (ROM) that contains 1024 × 32-bit input data of addr. In the proposed method we reduce the read-only memory (ROM) that contains 512 × 32-bit input data of addr, to decrease the area and delay of the existing method . The addr represents the data of four 32-bit Sboxes with 256 entries each. The 32-bit output data are read from the ROM at a positive clock edge. The proposed method can also lessen the total of slices used by the Blowfish design. A slice contains a set number of look-up tables (LUTs), FFs, and multiplexers. Thus, less logic resources are used to perform logic, arithmetic, and ROM functions that can lead to a faster encryption/decryption process [16].

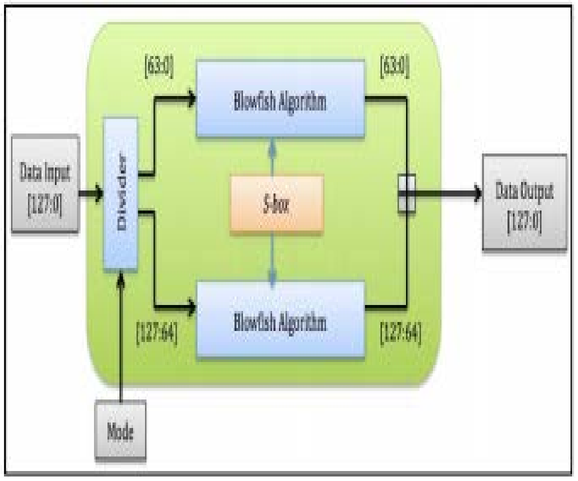
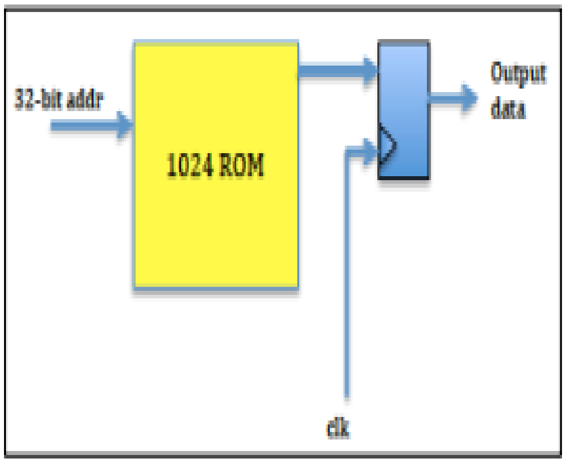
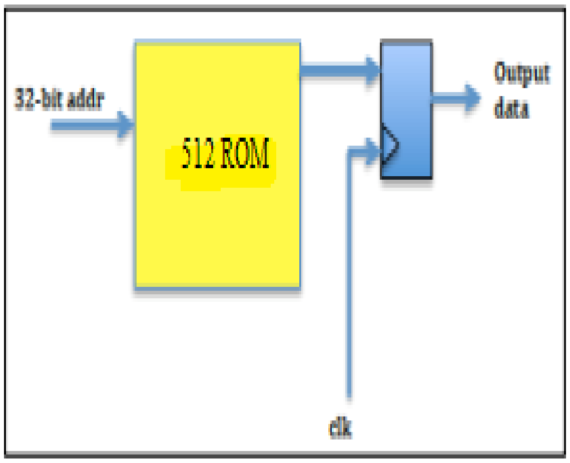


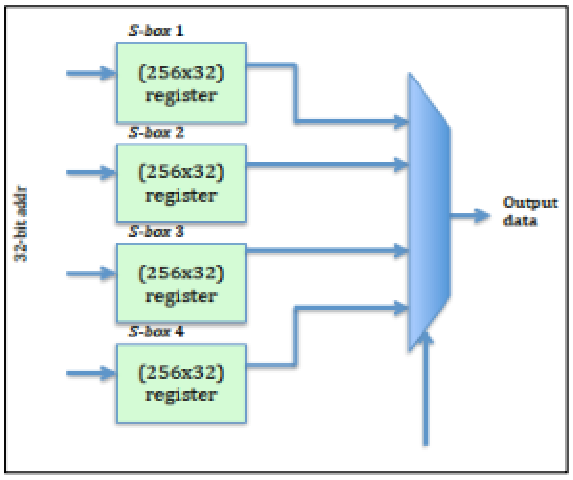
Figure 2: Block Diagram of the Proposed Blowfish Design.



(a) Existing Memory-based Method



(b) Proposed Memory-based Method



(c) Design Method by [12]

Figure 3: Schematic Comparison of Different Methods for S-boxes.

The proposed method is compared with the S-box method invented by [12] as shown in Fig. 3(b), since their output results are the best among others. The 256 × 32-bit registers are used for each S-boxes, which means the involvement of many groups of FFs that store a bit pattern. A single register has a clock, input data, and output data, and it enables a signal port. The 32-bit input data of addr are latched and stored internally for every clock cycle. This method can slow down the speed of the Blowfish performance as each register has its own timing delay.

IV. Throughput

Throughput is defined as the average rate of successful message delivery over a communication channel. In this paper, throughput is directed toward evaluating each architecture's characteristic and performance. Throughput is calculated as Eq. 1 based on [18].

Throughput (Gbps) = 128 bits * Clock Frequency (MHz)/Latency (1)

Latency is the encryption/decryption time that is calculated in clock cycles. Latency should be as small as possible to achieve a power-saving system. Furthermore, a long battery life is necessary, particularly for mobile devices.

For the proposed Blowfish, the achieved throughput is 2183 Mbps, which is 29% higher than the output result in [12]. The latency for each encryption and decryption mode is 19 clock cycles. Figure 4 shows the performance comparison between the proposed Blowfish design and previous studies. The proposed Blowfish is clearly the fastest with the smallest design size.

V. Conclusion

This paper presents a development of an improved power throughput Blowfish as a security algorithm, which is best embedded in mobile devices for wireless communication. Seven papers from previous studies are compared with the proposed Blowfish, and the performance is verified through reprogrammable FPGA. The optimal performance is defined strictly by the least number of hardware requirements, highest throughput, and lowest power consumption. The output results presented in this paper indicate that the proposed Blowfish has the smallest design core and highest throughput, with low power consumption. These findings prove the superiority of the proposed Blowfish design. These characteristics are necessary for current research trends given that the data need to be transmitted with a high speed using a low power source for energy efficiency.

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