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Symmetric transparent BIST for memory using March X algorithm

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Abstract

Symmetric Transparent BIST schemes for RAM modules assure the preservation of the memory contents during periodic testing while at the same time skipping the signature prediction phase required in transparent BIST schemes, achieving considerable reduction in test time. In this work the utilization of accumulator modules comprising adders implementing binary addition is proposed and BIST is implementing with Symmetric March X algorithm.

Keywords: online BIST, symmetric, SOC

1. INTRODUCTION

A March algorithm [1] consists of n march elements, denoted by Mi, with 0 ≤ i < n. Each March element comprises zero (or more) write operations, denoted by w0 / w1 (denoting that 0 / 1 is written to the RAM cell) and zero (or more) read operations denoted by r0 / r1, (i.e. 0 / 1 is expected to be read from the memory cell). For example, the C- algorithm (Figure 1(a)) consists of six March elements denoted by M0 to M5 [2]-[4].

In Figure 1, ⇧ denotes an increasing addressing order (which can be any arbitrary addressing order) and ⇩ denotes a decreasing addressing order (which is the inverse addressing order of ⇧).

M_0.	⇑ (w_0);	⇑ $((r_a)^c)$;
M_1.	⇑ (r_0, w_1);	⇑ (r_a, w_a^c);
M_2.	⇑ (r_1, w_0);	⇑ (r_a^c, w_a);
M_3.	⇓ (r_0, w_1);	⇓ (r_a, w_a^c);
M4.	⇓ (r_1, w_0);	⇓ (r_a^c, w_a);
M_5.	⇓ (r_0);	⇓ (r_a);
	(a)	(b)

Figure 1: C- March algorithm (a) original version (b) symmetric transparent version

In *transparent* BIST [5] the initial w0 phase is bypassed, and a "signature prediction" phase is used instead. The signature prediction phase consists of read operations equivalent to all the read operations of the March algorithm and it is utilized in order to calculate a signature that will be compared against the compacted signature calculated during the (remaining) march test.

Transparent BIST has the disadvantage that the signature prediction phase adds up to the total testing time with a percentage of (more than) 30%. In order to confront this problem, Yarmolik *et al* [6], [7] introduced the concept of symmetric transparent BIST.

In order to derive a symmetric transparent algorithm, the march series is modified in such way that the expected output response is equal to a known value [8]. In Figure 1(b) the ⇧ symmetric transparent version of the C algorithm is presented.

The notation for the transparent versions of the algorithms differs from the one used in traditional march algorithms. Instead of r0, r1, w0, w1, the notations r_a, r_a^c, w_a, w_a^c and $(r_a)^c$ are utilized. Their meanings are clarified in the following Table.

Notation	Meaning
r_a	Read the contents of a word of the RAM, expecting to read the initial contents of the RAM word (i.e. before the beginning of the test)
r_a^c	Read the contents of a word of the RAM, expecting to read the complement of the initial contents of the RAM word
$(r_a)^c$	Read the contents of a word of the RAM expecting to read the initial word contents and feed the complement value to the compactor
w_a	Write to the memory word; the value that was stored in this memory word at the beginning of the test is (assumed to be) written to the word.
w_a^c	Write to the memory word; the inverse of the value that was stored in this memory word at the beginning of the test is (assumed to be) written to the word.

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2. Rotate carry addition and accumulation

A rotate carry adder comprises a binary adder and a flip flop driven by the output of the carry output of the adder and driving the carry input. The operation performed is given by (1)-(2), where Din is the input of D and D is the output of D.

Out = In1 + In2 + D … (1)

Din = (In1+ In2 + D) mod 2n… (2)

The next (n+1)-bit state of an accumulator after state B|V if n-bit pattern P is applied, is given by N = V + P + B

The proposed scheme is based on the following Theorem, provided here without proof due to space limitations

Theorem:

If we start from the 0|(1)n state and apply a symmetric sequence to the inputs of the accumulator, the final state will be equal to the initial, i.e. 0|(1)n provided that the not all the contents of the memory are equal to the all-zero value. From Theorem 1, in order to apply symmetric transparent BIST in an n-word RAM, we can utilize an n-stage accumulator with rotate carry adder initialized to the state 0|11…1 and apply the symmetric transparent test using the accumulator as compactor of the responses, as will be shown in the next Section.

3. Symmetric transparent BIST with accumulators comprising rotate carry adders

Let us consider a 3-stage accumulator comprising a binary adder as shown in Figure 2(a). The 'B' inputs of the adder are driven by the output of the register (R) of the accumulator. The 'A' input is driven by the data output of the RAM as shown in Figure 2(c). The carry output of the adder is driven into the inputs of a flip flop whose output drives the carry input of the low-stage of the accumulator. In Figure 2 (b) the proposed scheme is presented. A series of XOR gates at the inputs of the 'A' input of the adder can invert the 'A' input depending on the value of the 'zero' signal; The 'B' inputs are driven by a series of AND gates gated by the 'zero' signal; zero is also driven to the carry input of the adder. The operation of the scheme of Figure1 (b) is presented in Table 1 with respect of the implementation of the various March operations.

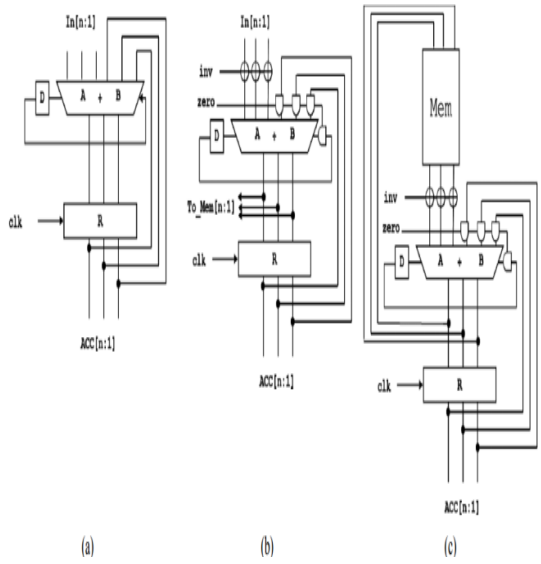


Figure 2: (a) Accumulator with Rotate carry adder (b) proposed scheme for compaction of the memory outputs (c) complete architecture

In Table 1, in order to implement operation (ra)c the inputs are complemented (inv = 1) and (since zero = 1) is added to the 'B' input i.e. the previous value of R. In order to perform the ra operation, in v is disabled and the content of the memory word is added to the value of R. In a similar way, in order to implement wac (in this way clk is disabled), the word is inverted and the added to the all-zero vector (since zero = 0).

Table 1: Operation of the proposed architecture

March operation	clk	inv	zero	'A' input	Input to Mem
$(ra)^c$	En	1	1	$(M[A])^c$	
ra	En	0	1	M[A]	
wa^c	Dis	1	0	$(M[A])^c$	$(M[A])^c$
ra^c	En	0	1	M[A]	
wa	Dis	1	0	M[A]	M[A]

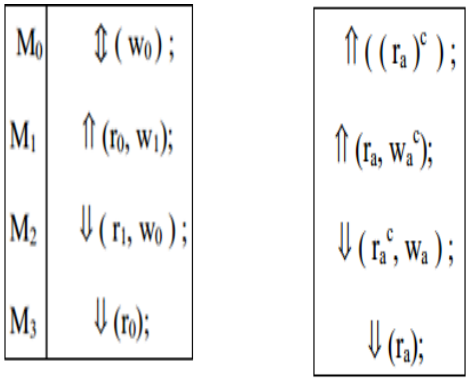
4. Proposed algorithm: March X algorithm:

Traditional March X Algorithms:

A March algorithm consists of *n* march elements, denoted by *M*i, with ($0 \leq i < n$). Each march element

comprises zero (or more) write operations, denoted by *w0/w1,* meaning that 0/1 is written to the RAM cell, and zero (or more) read operations denoted by *r0/r1,* meaning that 0/1 is expected to be read from the memory cell.

The March X algorithm [Fig. 3(a)] consists of four March elements denoted by *M*0 to *M*3. In Fig. 1, ⇑ denotes an increasing addressing order (which can be any arbitrary addressing order) and ⇓ denotes a decreasing addressing order (which is the inverse addressing order of ⇑).



(a) (b)

Figure 3: (a) Traditional March X algorithm, (b) Symmetric March X algorithms.

5. Simulation and Synthesize Results:

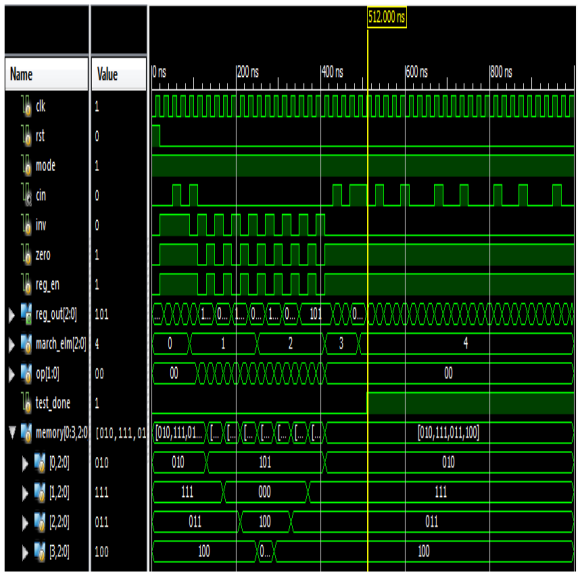


Figure 4: simulation results BIST with march X algorithm with symmetric

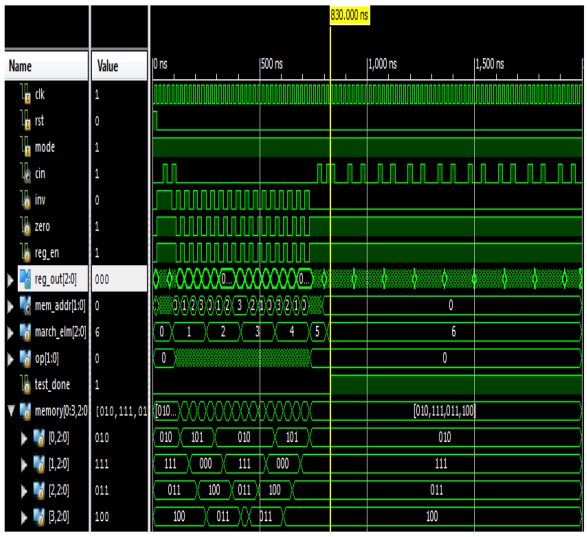


Figure 5: simulation results of BIST with March C algorithm with symmetric

Area comparison table:-

	March C Algorithm	March X Algorithm
Number Of Slices	**33**	**23**
Number of 4 input LUTs	**77**	**49**

Delay comparison table:-

	March C Algorithm	March X Algorithm
Delay	**5.8**	**5.1**

6. Conclusion

In this work we have presented a scheme for the testing of RAM modules using the symmetric transparent principle and accumulator modules comprising adders implementing binary addition is proposed. The proposed scheme tests a RAM with Symmetric transparent online BIST with March X algorithm.

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