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Design and Implementation of a Pipelined 64 bit MAC Unit with Vedic Multiplier and Reversible DKG Gate

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Abstract

The MAC unit which is drawn most importance in the DSP, has to concerned at much greater part. Optimizing the MAC unit plays a major role in DSP applications, optimizing the MAC require to cut down the two parameters: Power and Latency. The design of the MAC unit is based on the Vedic multiplier and the Reversible DKG gate. The Vedic multiplier is designed with the ancient Indian mathematics based on Atharvana Veda called "Urdhva Triyakbhyam. The adder unit is design with the Reversible Logic DKG adder. The reversible logic is one of the emerging out technology which is the future of Quantum computing. It has the advantage of least power consumption. The increasing trends in the VLSI and Low power design have increased the need of low power dissipation circuits to be designed. The Vedic Multiplier has the advantage of generating the partial products with reduce number and decreasing the latency. The 64 MAC unit design is programmed using Verilog - HDL using Xilinx ISE 14.7. The FPGA implementation is done on Spartan3E.

Keyword: Vedic multiplier, Reversible DKG gate component, Urdhvariyakbhayam.

1. INTRODUCTION

The multiplying algorithm used in DSP has to be design in taking into account of two factors: one the latency the second is throughput. These two factors are considered in perspective of delay. Latency gives the overall delay for the computation of the function. It is the time required to produce the stable output after the application of the stable inputs. Throughput gives the idea of how many multiplication operations can be carried out in a given amount of time. In designing MAC unit multiplying block is the unit which dissipates more amount of power, so to reduce the power consumption and delay various techniques has to be included in the design. The loss in the digital design is not entertained and considered to be one of the major issues. Various levels of integration and fabrication have reduced power consumption. One of the most promising approaches is the Reversible logic. Bennett proposed that the energy dissipated in any system is directly proportional to the amount of information lost or the number bits erased.

The design with the less number of information lost is Reversible logic. Reversible circuit/gate should be capable of generating a unique output from each input, and vice versa, i.e., there should be a one to one correspondence between the input and output vectors. As the number of output in a reversible gate or circuit has the same as the number of inputs, and one used is traditional NOT gate as reversible gate. Hence the reversible gate is always designed in say k x k manner, where k- input and k-output. The importance of the reversible logic is that it aims in achieving the minimum quantum cost. It is the number of logic gate required for the construction of the circuit.

2. LITERATURE SURVEY

MAC Unit

A multiplying function can be carried out in three ways: partial product Generation (PPG), partial product addition (PPA), and final conventional addition. The two bottle necks that should be considered are increasing the speed of MAC are partial product reduction and accumulator block. The 32 bit Mac design by using Vedic multiplier and reversible logic gate can be done in two parts. First, multiplier unit, where a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra.

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Multiplication is the fundamental operation of MAC unit [1]. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc. There are two major criterion that improve the speed of the MAC units are reducing the partial products and because of that accumulator burden is getting reduced. The basic operational blocks in digital system in which the multiplier determines the critical path and the delay. The (log2N + 1) partial products are produced by 2N-1 cross products of different widths for N*N. The partial products are generated by Urdhava sutra is by Criss Cross Method. The maximum number of bits in partial products will lead to Critical path.

The second part of MAC is Reversible logic gate. In modern VLSI, fast switching of signals leads to more power dissipation. Loss of every bit of information in the computations that are not reversible is kT*log2 joules of heat energy are generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In recent years, reversible logic functions has emerged and played a vital role in several fields such as Optical, Nano, Cryptography, etc.

3. MAC ARCHITECTURE

The proposed architecture has a MAC unit which is incorporated with a fastest acting Vedic multiplier in the data path and the multiplied output of the Vedic Multiplier is fed back into the Reversible adder which is initially reset. The final result obtained after the partial products addition is stored in the Accumulator register. The Fig 1 shows the Basic MAC unit based on the Vedic multiplier with the reversible adder built using Urdhva Triyakbhyam sutra with adder designed using DKG reversible logic gate is fitted to the MAC architecture. In order to improve the speed of the MAC unit there are two major bottlenecks. The first is the partial products reduction network and that is used in multiplication block and the second is the adder in the accumulator. Vedic Mathematics is originated from the ancient Indian arithmetic sutras. This derives from the Vedas. It was discovered in twentieth century. The name Vedic mathematics has its roots with total of sixteen principles, they are named as sutras. The Vedic multiplier used in the proposed design is based on one of the popular multiplication sutra called "Urdhva-Triyakbhyam".

The proposed MAC architecture is further divided into three modules:

1. Design of 64-Bit Vedic Multiplier using Urdhva Triyakbhyam sutra.
2. Design of DKG gate using reversible logic.
3. Accumulator design which integrates both the Vedic multiplier and reversible adder.

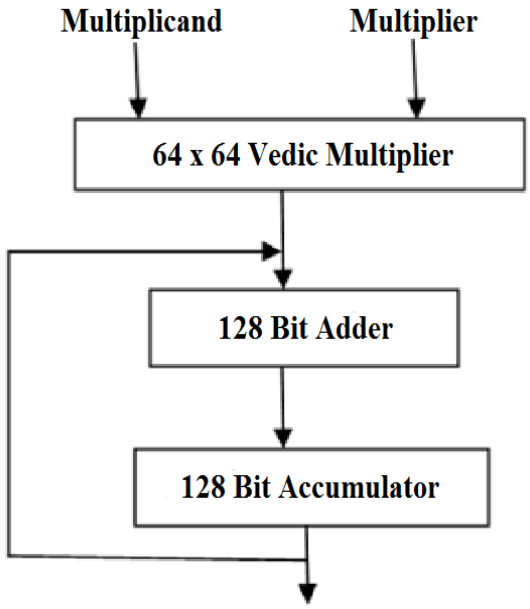

Figure 1: Proposed MAC Unit Design

4. MAC 64 X 64 Pipelining Architecture:-

The architecture has a pipelining MAC unit which is incorporated with a fastest acting Vedic multiplier in the data path and the multiplied output of the Vedic Multiplier is fed back into the Reversible adder which is initially reset. Here we can introduce the registers in different stages to increase the total performance of MAC Unit. The final result obtained after the partial products addition is stored in the Accumulator register. The Fig 2 shows the pipelining MAC unit based on the Vedic multiplier with the reversible adder built using Urdhva Triyakbhyam sutra with adder designed using DKG reversible logic gate is fitted to the MAC architecture.

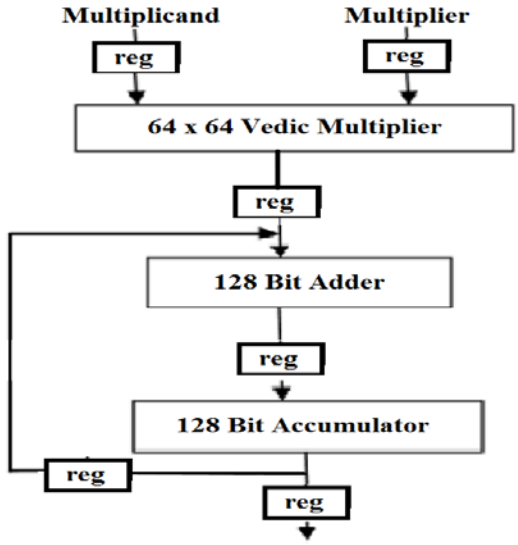

Figure 2: Proposed MAC Unit with Pipelining Design

A. 64 X 64 Vedic Multiplier:-

Fig 6 shows the 64 x 64 Vedic multiplier. With referring to the figure it is easy to understand that the Vedic multiplier has to be designed by following the hierarchical method. The design of the Vedic multiplier requires the lower level bit multiplier say 32 x 32 bit for the design of 64 x 64 Vedic multiplier. The design further requires 16, 8, 4 and finally the 2 bit multiplier. Hence it is easy to extend the multiplier architecture to the higher level by keeping its modularity. The design requires the intermediate adder stage. The adder stage it of the reversible logic adder design using one of the most popular reversible gate DKG gate. The two number A and B are applied in the crosswise order. The inputs are of 64 bit and final result will be maximum of 128 bit. The logic behind the operation of the architecture is the given number which is of 64 bit is sub divided into two halves each of 32 bit. The input to the first stage of multiplier will be lower halve of both the numbers, second and third stage will be swapped halves of the two and the final and fourth stage will be the upper half of the numbers. The multiplication operation is followed by the addition operation which can add 64 bit numbers and the sum will be saved, the carry if generated will be added to the next successive stages and so on. The adder will be appended with zeros to one of the input in order to equate the number of bits so as the addition operation can be performed without any error. Three DKG adder stage can be rectified by inspecting the architecture of the 64 bit multiplier. The adder is responsible to provide the carry o0f the last stage where the output of the last stage adder is considered as the sum. The LSB sum bits will be directly taken from the first stage of the multiplier. The architecture has the 32 bit multiplier whose architecture is the photocopy of the 64 bit multiplier except the difference is the 32 bit architecture consists of the inputs to be 32 bits and the Reversible DKG adder of 32 bit. Ca in the architecture refers to the carry generated in that particular stage of operation.

B. 2X2 Vedic Multiplier:-

The 2x2 multiplier has the multiplier and multiplicand to be of 2 bits. It gives maximum of bits as result in terms of sum and carry. The inputs may be of any one combination from 00 to 11. (00, 01, 10, 11). The output lies between: 0000, 0001, 0010, 0011, 0110 and 1001. By using the Vedic sutra for multiplication, the 2 bit Vedic multiplier.

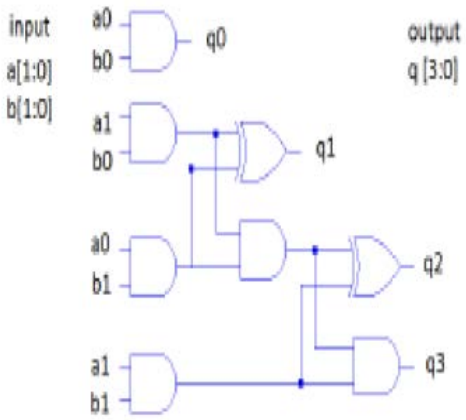

Figure 3: Hardware realization of 2x2 Vedic multiplier

C. 4X4 Vedic multiplier:-

The next level in the design will be the 4 bit Vedic multiplier design. It requires the 2x2 multiplier design, the input multiplicands will have maximum of 4 bit which ranges from 0000, 0001, 0010…….1111. The output produced will be of 8-bit, the Vedic multiplier improvised algorithm states that the Vedic multiplier should have 4 input multiplier where the inputs will be applied in the vertical and crosswise order.

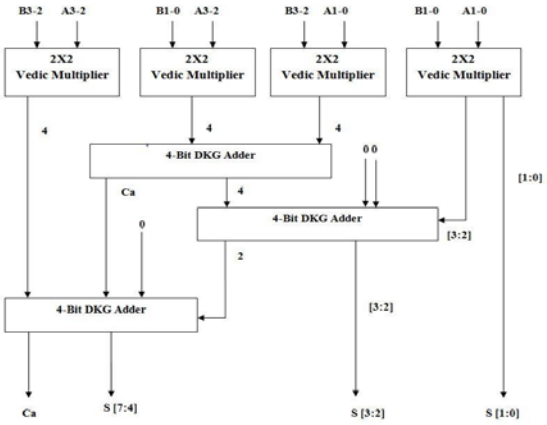

Figure 4: Hardware realization of 4x4 Vedic multiplier

D. 32x32 Vedic Multiplier:-

The 32x32 multiplier design has the 16x16 Vedic multiplier design. The logic of the block diagram remains the same based on the improvised Vedic Sutra. Here both the multiplicands will be of 32 bits. (m=32). The multiplicands have to be divided into 2 according to the improvised algorithm. The result of the 16x16 multiplication will be maximum of 32 bits. The inputs A and B are divided into two halves each of 16 bits (m/2). The 32 bit multiplier input ranges from B0, B1 ……B32.

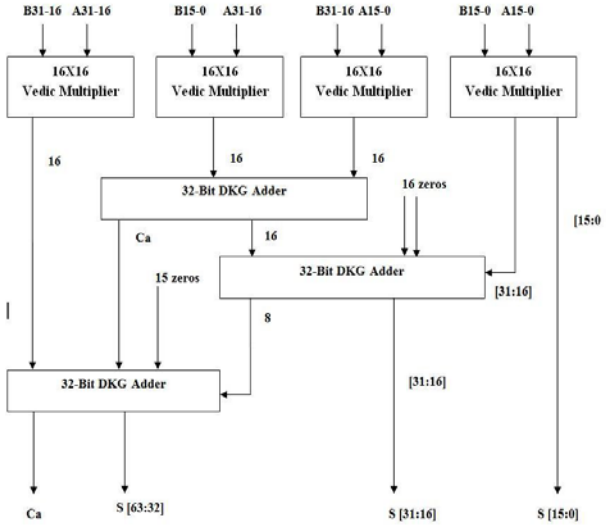

Figure 5: Hardware realization of 32x32 Vedic multiplier

E. 64x64 Vedic Multiplier:-

The 64x64 multiplier design has the 32x32 Vedic multiplier design. The logic of the block diagram remains the same based on the improvised Vedic Sutra. Here both the multiplicands will be of 64 bits. (m=64). The multiplicands have to be divided into 2 according to the improvised algorithm. The result of the 32x32 multiplication will be maximum of 64bits. The inputs A and B are divided into two halves each of 32 bits (m/2). The 64 bit multiplier input ranges from B0, B1 ……B63.

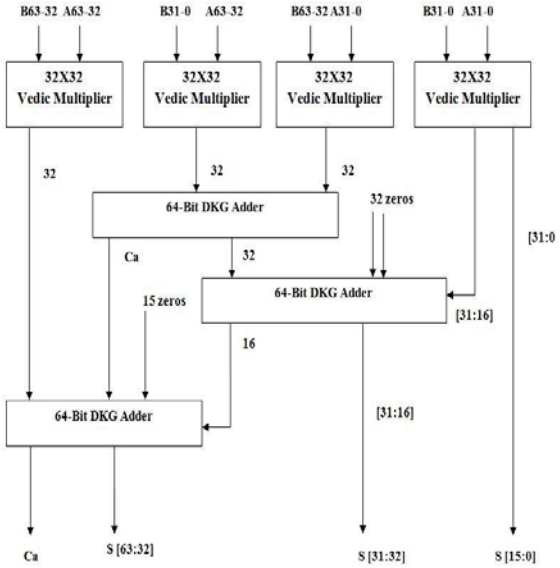

Figure 6: 64 x 64 Vedic Multiplier Architecture

5. Design of Adder Using Reversible Logic DKG Gate

A. Reversible logic

Reversible logic is a unique technique (different from other logic). Loss of information is not possible in here. In this, the numbers of outputs are equal to the number of inputs.

a. General consideration for reversible logic gate :-

A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer [18] proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet [17] showed that a circuit consisting of only reversible gates does not dissipate power. In the design of reversible logic circuits, the following points must be kept in mind to achieve an optimized circuit:

- Fan-out is not permitted
- Loops or feedbacks are not permitted
- Garbage outputs must be Minimum

- Minimum delay
- Minimum quantum cost
- Zero energy dissipation [17]

b. DKG Gate

A 4* 4 reversible DKG gate [6] that can work singly as a reversible full adder and a reversible full subtractor is shown below. If input A=0, the DKG gate works as a reversible Full adder, and if input A=1 then it works as a reversible Full subtractor. It has been verified that a reversible full-adder circuit requires at least two or three garbage outputs to make the output combinations unique [5], [6].

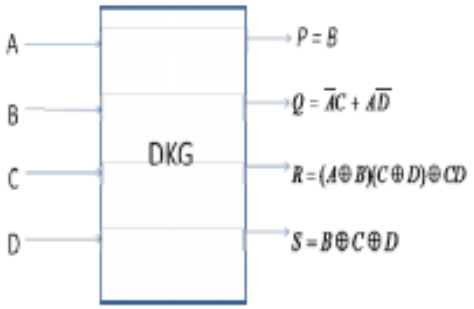

Figure 7 (a) DKG gate

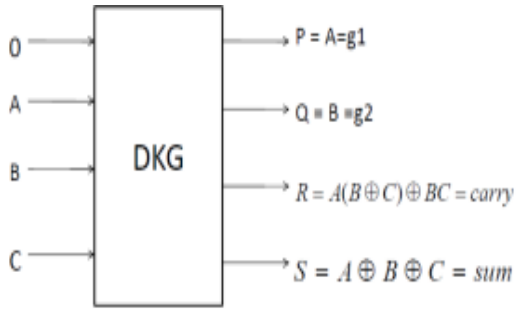

Figure 7 (b) DKG gate as a Full adder

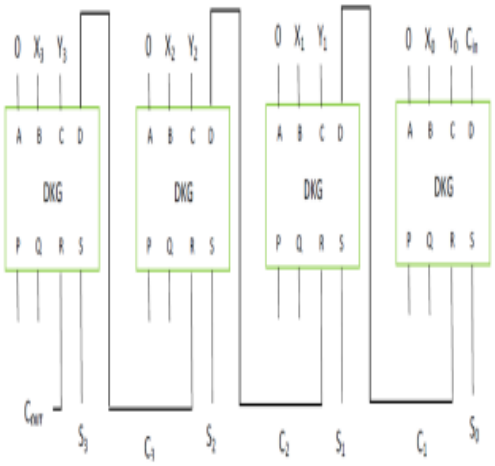

Figure 7 (c) Parallel adder using DKG gate

6. Accumulator Stage

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using our design had better performance when compared to the pervious MAC designs.

7. Simulation And Synthesies Results:-

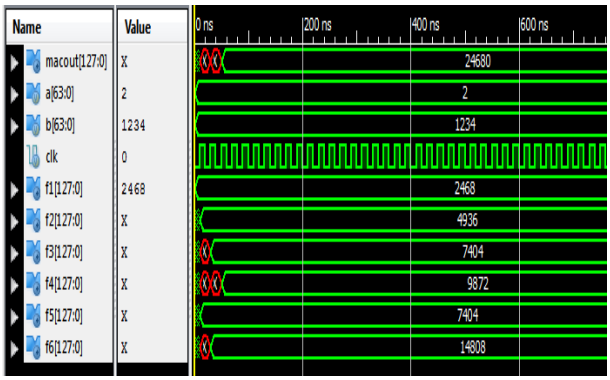

Figure 8: Simulation output of 64 bit MAC Design

Table 1: DELAY REPORT FOR MAC 64 X64 UNIT WITH PIPELINING AND WITH OUT PIPELING:-

	MAC with out pipelining	MAC with pipelining
Delay	**938.251 ns**	**60.897**

8. Conclusion:-

The MAC unit should have the fastest available output with the less amount of power consumption and the area has to minimize. The Design satisfies the condition of being the optimized design which can be replaced in future application of DSP such as DCT (Discrete Cosine Transform), DFT (Discrete Fourier Transform) etc.; The Vedic multiplier has the property

of minimizing the delay in propagation and the DKG gate with the advantage of lower power consumption.

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