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Design of Optimized Radix-2 and Radix-4 Butterflies from FFT with Decimation in Time

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Abstract

In the FFT computation, the butterflies play a central role, since they allow calculation of complex terms. In this calculation, involving multiplications of input data with appropriate coefficients, the optimization of the butterfly can contribute for the reduction of power consumption of FFT architectures. In these paper different and dedicated structures for the 16 bit-width radix-2 and radix-4 DIT butterflies are implemented, where the main goal is to minimize the number of arithmetic operators in order to produce power-efficient structures. Firstly, we improve a radix-2 butterfly previously presented in literature, reducing one adder and one subtractor in the structure. After that, part of this optimized radix-2 butterfly is used to reduce the number of real multipliers in the radix-4 butterfly. The main results show that the optimization guarantees reduced power consumption for radix-2 butterfly, when compared with previous works from the literature. Moreover, the use of part of the optimized radix-2 into the radix-4 structure leads to the reduction of power consumption for this structure.

Keywords: FFT; Radix-2 butterfly; Radix-4 butterfly; power consumption reduction

INTRODUCTION

Fast Fourier Transform (FFT) is the largely implementation of the Discrete Fourier Transform (DFT), because this algorithm needs less computation due its recursive operator named butterfly. This operator performs the calculation of complex terms, which involves multiplication of input data by appropriate coefficients [1]. In [2], a radix-2 butterfly structure, with Decimation in Time (DIT), based on four multipliers, and three other structures based on three multipliers, for the calculation of the real and imaginary parts are presented. A new structure, also based on three multipliers, was presented in [3]. Among the structures of [2], and [3], the original structure (named structure A), based on 4 multipliers, presented the best power consumption result. However, one of the three multiplier based structures (named structure B) proved to be potentially power consumption reduction, mainly when two levels of pipeline was used, because it enabled the reduction of one multiplier, and because the large reduction of the critical path. In this work, we optimize the radix-2 butterfly structure B from [2] by changing the positions of the operands and the twiddle factors inside the architecture, what enables the reduction of two adder/subtractor circuits. According to [4], radix-4 algorithms have a computational advantage over radix-2 algorithms because one radix-4 butterfly does the work of four radix-2 butterflies, and the radix-4 butterfly requires only three complex multipliers compared to four complex multipliers of four radix-2 butterflies. In this work, the focus is to reduce the number of real multipliers in the radix-4 DIT butterfly, whose original structure is composed of 12 real multipliers to compute one complex multiplication. As will be presented later, when using part of the proposed optimized radix-2 butterfly, the radix-4 butterfly has reduced three real multipliers inside its structure. The radix-2 and radix-4 butterflies were implemented in hardware description language, with 16-bit width, and synthesized to 45nm Nan gate Open Cell Library [5] using Cadence Encounter RTL Compiler version 8.10 synthesis tool [6]. Area, delay, and power values for the dedicated butterflies structures are presented. The main contributions of this work are: The optimization of the radix-2 butterfly from the literature; The optimization of the radix-4 butterfly by implementing it using part of the optimized radix-2 butterfly. The rest of the document is organized as follows. The next section makes an

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overview of relevant work related to our own. In Section III we present the main aspects of the radix-2 and radix-4 butterflies from FFT algorithm with Decimation in Time. In Section IV we present the implemented structures of the butterflies. Area and power results for the butterflies obtained from the logic synthesis tool are presented in Section V. Finally, in Section VI we conclude this paper, discussing the main contributions and some ideas for future work.

RADIX-2 AND RADIX-4 WITH DECIMATION IN TIME OVERVIWEW

The main goal of the FFT algorithms is to compute the Discrete Fourier Transform efficiently [13]. The FFT X(k) of a signal x(n) can be computed using (1), where WN is named twiddle factor, i is the imaginary component and N is the number of points of the FFT. The FFT has a hierarchical computation and the butterfly plays a central role in this computation [1].

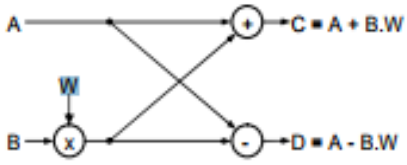
$$X(k) = \sum_{n=0}^{N-1} x(n).W_N^{k.n}$$

$$W_N = e^{-i2\pi/N} \qquad (1)$$

$$0 \leq k \leq N-1 \;\&\; 0 \leq n \leq N-1$$

Radix-2 Butterfly:

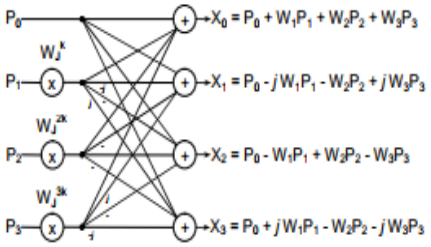
For the radix-2 FFT algorithm with decimation in time, the butterfly allows the calculation of complex terms according to Fig. 1. According to the structure shown in Fig. 1, the butterfly is composed of addition, subtraction and multiplication, where these operations involve complex numbers. In this work, two alternative butterfly structures from the literature and one proposed optimized structure are presented to perform these complex numbers operations.



Structure of DIT radix-2 butterfly.

Radix-4 Butterfly

The flow of the radix-4 DIT butterfly is presented in Fig. 2 [4]. Note that the radix-4 butterfly requires three complex multipliers for the computation of the complex inputs. Therefore, one radix-4 butterfly does the work of four radix-2 butterflies [4]. In this work, the radix-4 butterfly was implemented by using part of our optimized radix-2 butterfly, as will be presented in the next section.



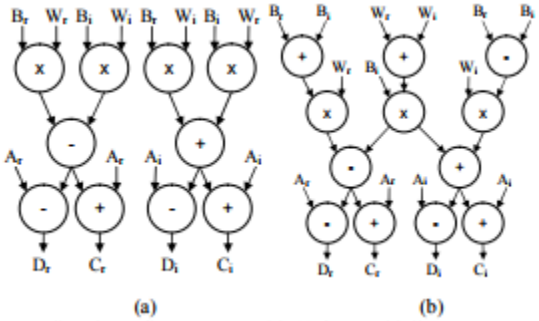
Structure of DIT radix-4 butterfly

OPTIMIZED RADIX-2 AND RADIX-4 BUTTERFLIES STRUCTURES

This section presents the radix-2 DIT structures from the literature, introduces the radix-4 DIT structures, and presents the proposed optimizations for both structures.

Radix-2 Butterfly Structure

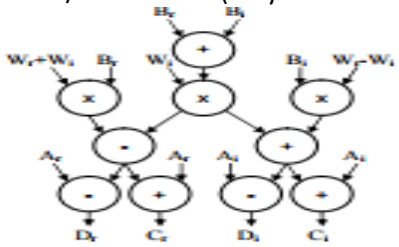
Fig. 3 presents the structure A (a) and the structure B (b) of radix-2 butterfly with four and three multipliers, respectively [2],[3]. Note that even with the reduction of one multiplier, the structure B presents three more adder/subtractor operators than the structure A.



Radix-2 butterfly structures with (a) four multipliers - Structure A, and with (b) three multipliers - Structure B

By keeping the structure B under close observation, it was possible to note that swapping the inputs order of the operand B and the twiddle factor W, it is possible to optimize the amount of arithmetic operations. In fact, with this reordering, two arithmetic operations between the twiddle factors W can be avoided, since the operations can be previously realized and stored in memory. This simplification leads to the reduction of one adder and one subtractor in the structure B, as can be seen in Fig. 4. Therefore, the optimized structure B presents one multiplier less than the structure A,

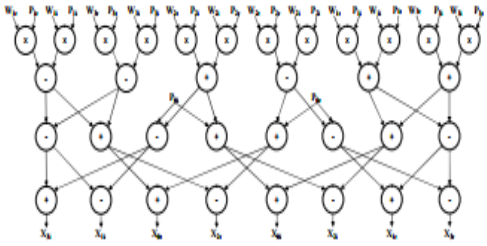
with almost the same number of adders/subtractors (only one more adder).



Optimized DIT radix-2 butterfly of Structure B

Radix-4 Butterfly Structure

As could be observed in Fig. 2, the radix-4 DIT butterfly is composed of three complex multipliers, as well as the other needed complex adder and subtractors. The development of the complex equations of Fig. 2, and the grouping of the terms into real and imaginary parts, leads to the structure of Fig. 5, with 12 multipliers and 22 adders/subtractors.

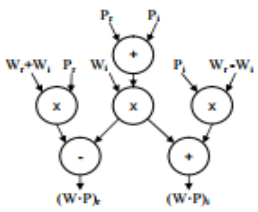


Radix-4 butterfly structure

As the radix-4 structure is composed of three complex multipliers ($\cdot$, $\cdot$, $\cdot$), as presented in Fig. 2, thus we reused part of our optimized radix-2 butterfly in order to reduce the number of multipliers of the radix-4 butterfly. The equations for one complex multiplication ($\cdot$), separated into real and imaginary outputs, are presented in (2) and (3), respectively. The structure for these equations, in terms of real and imaginary multiplications and additions/subtraction is presented in Fig. 6.

$$(W \cdot P)_r = [P_r \cdot (W_r + W_i)] - [W_i \cdot (P_r + P_i)] \quad (2)$$

$$(W \cdot P)_i = [P_i \cdot (W_r - W_i)] + [W_i \cdot (P_r + P_i)] \quad (3)$$



Structure for complex multiplication of two terms

The reuse of (2) and (3) into each multiplication term of the equations of Fig. 2, leads to the expressions (4)-(11

$$X_{0r} = P_{0r} + (W_1 \cdot P_1)_r + (W_2 \cdot P_2)_r + (W_3 \cdot P_3)_r \quad (4)$$

$$X_{0i} = P_{0i} + (W_1 \cdot P_1)_i + (W_2 \cdot P_2)_i + (W_3 \cdot P_3)_i \quad (5)$$

$$X_{1r} = P_{0r} + (W_1 \cdot P_1)_i - (W_2 \cdot P_2)_r - (W_3 \cdot P_3)_i \quad (6)$$

$$X_{1i} = P_{0i} - (W_1 \cdot P_1)_r - (W_2 \cdot P_2)_i + (W_3 \cdot P_3)_r \quad (7)$$

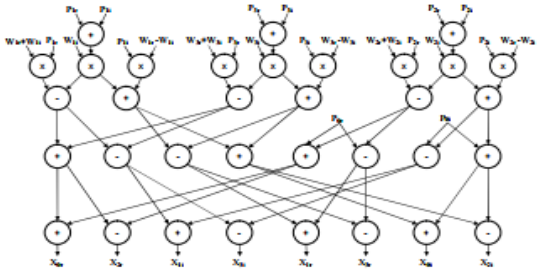
$$X_{2r} = P_{0r} - (W_1 \cdot P_1)_r + (W_2 \cdot P_2)_r - (W_3 \cdot P_3)_r \quad (8)$$

$$X_{2i} = P_{0i} - (W_1 \cdot P_1)_i + (W_2 \cdot P_2)_i - (W_3 \cdot P_3)_i \quad (9)$$

$$X_{3r} = P_{0r} - (W_1 \cdot P_1)_i - (W_2 \cdot P_2)_r + (W_3 \cdot P_3)_i \quad (10)$$

$$X_{3i} = P_{0i} + (W_1 \cdot P_1)_r - (W_2 \cdot P_2)_i - (W_3 \cdot P_3)_r \quad (11)$$

From (4)-(11), we have obtained an optimized radix-4 butterfly structure, with three fewer multipliers than the structure of Fig. 5, as can be seen in Fig. 7. Note that the reduction of the multipliers is obtained at the cost of the increase of three adders. However, as multipliers are more complex than adders, thus the proposed optimized radix-4 solution can be more power efficient, as compared with the solution of Fig. 5, as will be presented in the next section.



Optimized radix-4 butterfly structure.

CONCLUSIONS

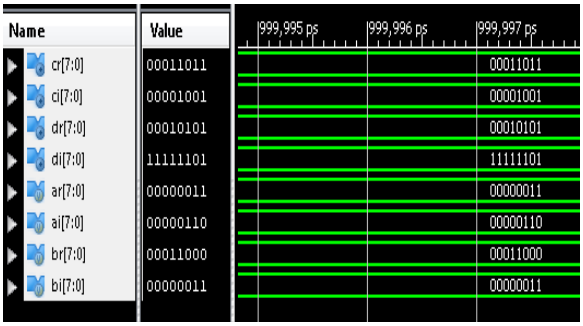
This work presented optimized radix-2 and radix-4 butterflies from FFT with Decimation in Time. The optimized radix-2 butterfly presented less power consumption than the solutions from the literature, because with the proposed optimizations was possible to reduce one adder and one subtractor in the architecture.

From the obtained results it was possible to note that, when using part of the optimized radix-2 butterfly, the proposed optimized radix-4 butterfly has been proved to be power efficient, when compared with the original one.

One important aspect to be emphasized is that the proposed optimizations in radix-2 butterfly enables the use of shift-adder circuits, rather than a complex multiplier from the tool, as we have used in this work. Therefore, as future work we intend to verify the impact on power consumption reduction, when using the shift/add-based radix-2 butterfly into the radix-4 butterfly.

Results:-

Simulation wave forms



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