

Design and implementation of Wallace tree multiplier using parallel prefix adder (Kogge Stone adder)

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Abstract

Fixed point Wallace tree multiplier architecture is used to perform multiple multiplications on different data paths. Wallace tree multiplier using Kogge Stone and Brent Kung adders perform more number of multiplications in parallel with fewer extra carry save adder stages than existing multiplier. The modified n-bit Wallace tree multiplier structure is used to perform four $(n/2) \times (n/2)$ -bit multiplications, two $n \times (n/2)$ -bit multiplications and one $n \times n$ -bit multiplication in parallel. In the existing Wallace tree multiplier design Carry lookahed adder (CLA) is used. To further improve the speed and to reduce the area parallel prefix adders are used in the modified Wallace tree multiplier. The Kogge Stone adder (KSA) is used for high-speed and Brent Kung adder (BKA) is used to reduce the area. Wallace tree multiplier using KSA and BKA are implemented using Xilinx 14.7

Keywords: Kogge stone adder, Brent Kung adder, Wallace tree multiplier.

INTRODUCTION

The performance of the embedded system, microprocessor and many modern DSP applications are mainly dependent on the performance of the multipliers as it is the key element. An efficient system can be build by making suitable multiplier for the system. A multiplier has two stages, partial product generation and partial product addition. An n bit multiplier produce n number of partial products and to reduce this number of partial products modified Booth algorithm [1] was used. But booth encoder in this multiplier increases the circuit depth. The n bit Baugh Wooly array multiplier [2] has the circuit depth $O(n)$. In modern technology, vector processors [3] are playing a major role to achieve data level parallelism (DLP). Here multiple operands are following the multiple data paths in the same hardware. So only one instruction is used to perform the operations on the vector of data. The twin precision based array multiplier is explained in [4] is used for data level parallelism. Where the full precision multiplier is used to implement two half precision multiplications with circuit depth of $O(n)$. That is the 8-bit multiplier is used to perform two 4-bit multiplications or one 8 bit multiplication at a time. The depth of Carry Save Adder (CSA) is $O(1)$. The depth of the carry save addition tree is $O(\log_2 n)$

for Wallace tree [5] based multiplier and $O(n)$ for Braun based [5] multiplier, where n is the number of bits. The quarter precision Wallace tree multiplier [6] is used to produce the multiple multiplications to improve the speed with increased circuit depth as trade off. To further improve the speed and reduce the area Wallace tree multiplier using Kogge Stone adder and Brent Kung adder [7]-[8] are used.

32-BIT WALLACE TREE MULTIPLIER

The modern digital signal processor requires large multiplier to compute complex signal processing operations. The DSP processor shows the need for 64-bit Multiplier, where four 32×32 -bit multiplications or sixteen 16×16 -bit multiplications or four 16×32 -bit multiplications or four 8×8 -bit multiplications are performed using one 64-bit Multiplier in parallel. In the same way, the Wallace tree multiplier architecture is allowed to perform more than one multiplication in parallel to achieve data level parallelism in vector processors. The 32-bit Wallace tree multiplier is having 8 carry save stages and 54-bit final adder to get the product. Where the modified 32-bit Wallace structure is having Block I, Block II, Block III and 25-bit recursive doubling based CLAs are involved. Fig. 3, 4 and 5 are showing the architecture for Block I, Block II and Block III respectively. Each of the Block I will act as 16-bit

Wallace tree multiplier's carry reduction tree and they are getting the partial products from each of the quarters. The Block I is having 6 carry save stages. The final carry and sum from CSA14 of Block I is sent to 25-bit CLA to get four 16-bit multiplication results at a time.

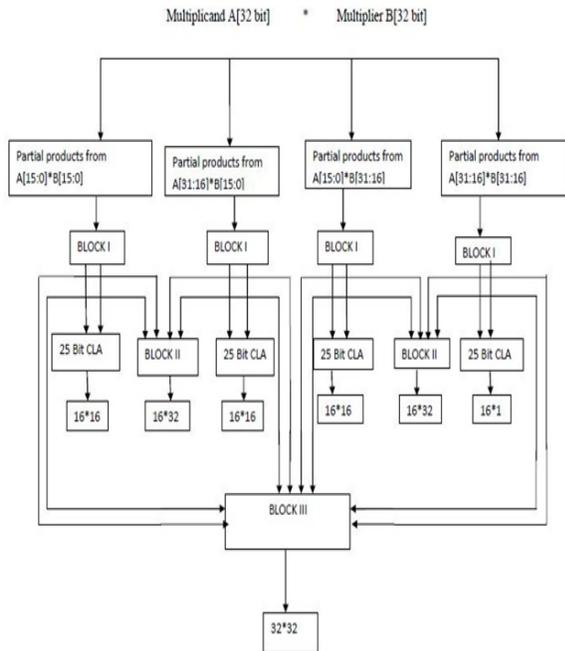


Fig.1: Wallace tree multiplier



Fig. 2: Partial product arrangement

Block III respectively. Each of the Blocks I will act as 16-bit Wallace tree multipliers carry reduction tree and they are getting the partial products from each of the quarters. The Block I is having six carry save stages. The final carry and sum from CSA14 of Block I is sent to 25-bit CLA to get four 16-bit multiplication results at a time.

A. Blocks of 32-bit Wallace tree multiplier

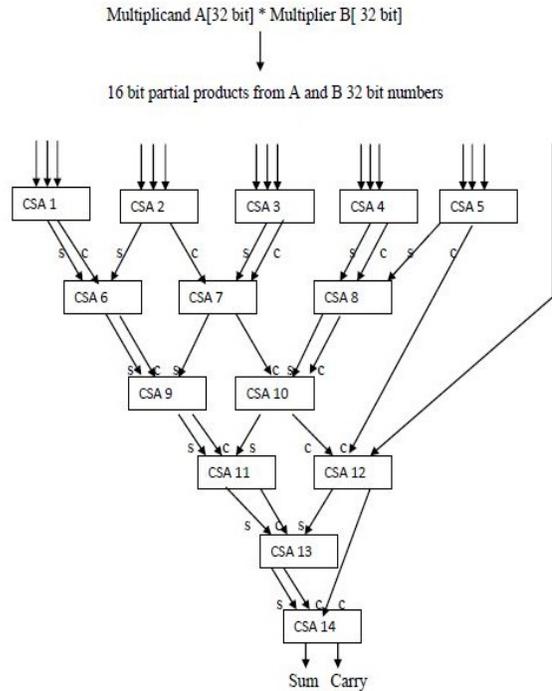


Fig.3: Block I of Wallace tree multiplier

Block II

The inputs to Block II are from the output of CSA14 of two of the Block I, which tends to produce two 16x32-bit multiplication results in parallel. The Block II is having two carry save stages and one 40-bit recursive doubling based CLA. Similarly the inputs to block III are from the output of CSA14 of the entire Block I, which tends to produce one 32x32-bit multiplication result. The Block III is having four carry save stages and one 54-bit recursive doubling based CLA. And all the Block II, Block III and 25-bit CLAs are in parallel. Therefore the critical path of the modified structure includes Block I and Block III. So the total critical depth of the 32-bit Wallace tree multiplier is equal to the addition of number of carry stages of Block I, number of carry save stage of Block III and depth of 54-bit recursive doubling based CLA. So the critical path of Wallace structure includes 10 carry save stages and one 54-bit recursive doubling based CLA. So the Wallace structure requires two extra carry save stages than existing 32-bit Wallace structure and these causes slightly increase in the worst path delay of modified system than the existing multiplier. The 32-bit Wallace structure has 30 carry save adders and one 54-bit recursive doubling based CLA. The Block I

has 14 Carry Save adders (CSA), Block II has 2 Carry Save adders and cell III has six Carry Save adders. So the 32-bit Wallace structure has $(4 \times 14) + (2 \times 2) + (1 \times 6) = 66$ Carry Save adders, four 25-bit recursive doubling based CLAs, two 40-bit recursive doubling based CLAs and one 54-bit recursive doubling based CLA. And hence, this huge difference causes increase in total cell area, total number of cells and net power than conventional structure.

Block III

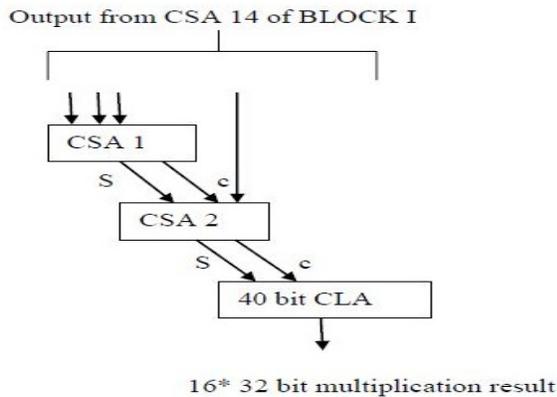


Fig. 4: Block II of Wallace tree multiplier

Block III

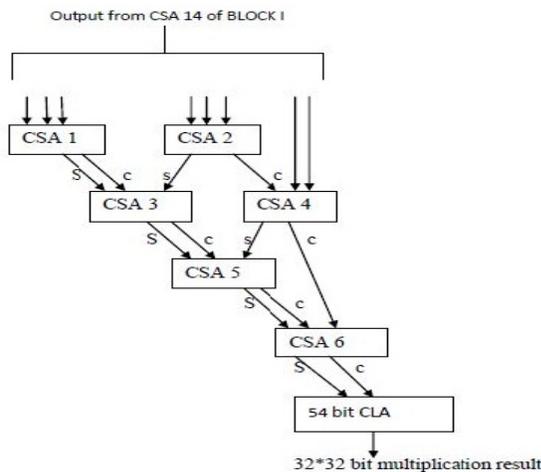


Fig. 5: Block III of Wallace tree multiplier

MODIFIED WALLACE TREE MULTIPLIER

In Wallace tree multiplier [6] CLA is replaced with Kogge Stone adder (KSA) and Brent Kung adder (BKA) to further improve the speed and reduce the area. Kogge Stone adder and Brent Kung adders are the parallel prefix adders. Parallel-prefix structures are found to be common in high performance adders

because the delay is logarithmically proportional to the adder width. The parallel prefix adders are more flexible and are used to speed up the binary additions. Parallel prefix adders are obtained from Carry Look Ahead (CLA) structure. The construction of parallel prefix adder involves three stages

1. Pre-processing stage
2. Carry generation network
3. Post processing

Pre-processing stage In this stage we compute, generate and propagate signals to each pair of inputs A and B. These signals are given by the logic equations 1&2:

$$P_i = A_i \text{ xor } B_i \tag{1}$$

$$G_i = A_i \text{ and } B_i \tag{2}$$

Carry generation network In this stage we compute carries corresponding to each bit. Execution of these operations is carried out in parallel. After the computation of carries in parallel they are segmented into smaller pieces. It uses carry propagate and generate as intermediate signals which are given by the logic equations 3 and 4:

$$CP_{i:j} = P_{i:k+1} \text{ and } P_{k:j} \tag{3}$$

$$CG_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j}) \tag{4}$$

Post processing This is the final step to compute the summation of input bits. It is common for all adders and the sum bits are computed by logic equation 5 and 6:

$$C_{i-1} = (P_i \text{ and } C_{in}) \text{ or } G_i \tag{5}$$

$$S_i = P_i \text{ xor } C_{i-1} \tag{6}$$

These parallel prefix adders contain gray cells and block cells. The black cell (BC) generates the ordered pair, the gray cell (GC) generates only left signal [7].

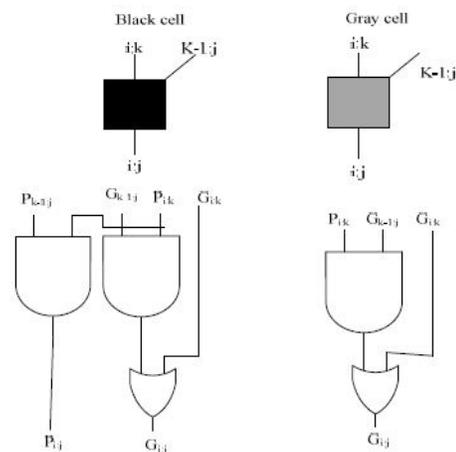


Fig.6: Black cell and gray cell

32 BIT WALLACE TREE MULTIPLIER USING KSA

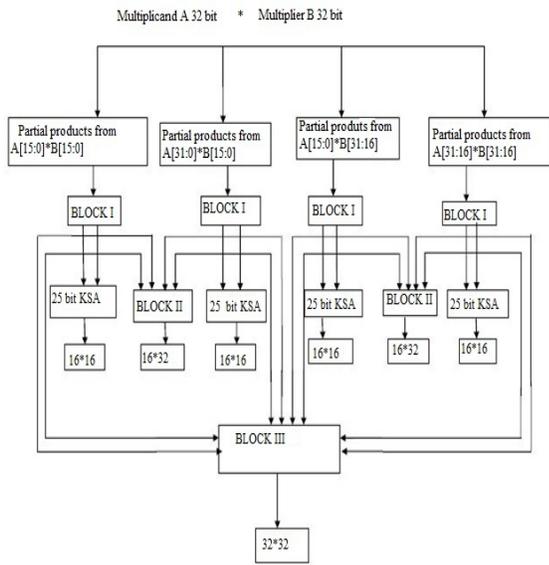


Fig. 7: Modified Wallace tree multiplier using KSA

Kogge-Stone adder is a parallel prefix form of carry look-ahead adder. A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is $O(\log n)$. It is a fastest adder design and common design for high performance adders in industry. In pre computation stage propagation and generation operations are performed. Stage1 used 14 black cells and one gray cell. Stage2 used 12 black cells and two gray cells. Stage3 used 8 black cells and 4 gray cells. Stage4 used 8 gray cells. In final computation stage sum and carry generated.

16-bit Kogge Stone adder

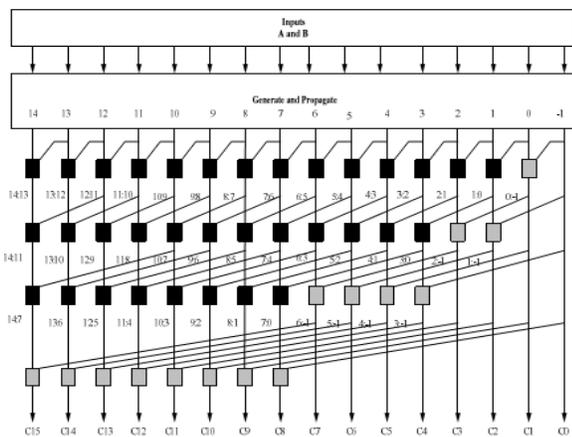


Fig. 8: 16-bit Kogge Stone adder

Block II

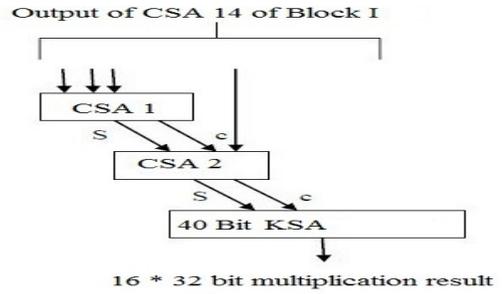


Fig. 9: Block II of modified Wallace tree multiplier using KSA

BLOCK-III

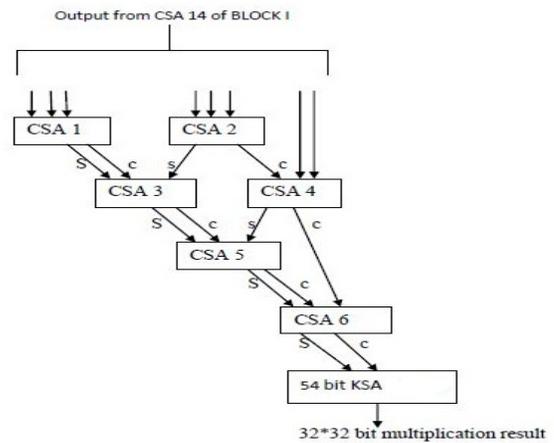


Fig. 10: Block III of modified Wallace tree multiplier using KSA

SIMULATION WAVEFORMS

Name	Value	0 ns	10 ns	20 ns	30 ns	40 ns	50 ns	160 ns
ll_res[31:0]	21491920	21715600	2628240	21491920				8
lh_res[31:0]	21491920	0	0	21491920				0
hl_res[31:0]	74560	0	0	74560				0
hh_res[31:0]	74560	0	0	74560				0
lm_res[47:0]	14085159610	21715600	2628240	14085159610				8
hm_res[47:0]	4886488720	0	0	4886488720				0
Final_res[63:0]	32164616393	21715600	2628240	32164616393				8
a[31:0]	305402420	4560	564	305402420				2
b[31:0]	1053188	4560		1053188				4

The simulation is done using Xilinx ISE 14.7 tool. In the above waveform a and b are 32-bit numbers. The final output is 64-bit multiplication result. In parallel four 16*16 bit and two 16*32 bit results also produced.

Table 1: COMPARISON OF DELAY OF WALLACE TREE MULTIPLIER USING ADDERS

Wallace tree multiplier type	Delay
Wallace tree multiplier using carry lookahed adder	80.977ns
Wallace tree multiplier using kogge stone adder	32.461ns

The delay of Wallace tree multiplier using Kogge Stone adder is improved from 80.977ns to 32.416ns.

CONCLUSION

A 32-bit Wallace tree multiplier is modified and redesigned. The modified Wallace tree multiplier achieves data level parallelism in vector processors. In addition part CSA, CLA adders used to enhance to prefix adders KSA. KSA adder having high-speed adder using 32 bit Wallace tree multiplier is implemented by Xilinx 14.7 and hardware kit FPGA spartan3e.

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