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Layout Design & Power Scaling Technique in 3D Integrated Circuits

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Abstract

A three-dimensional integrated circuit (3D IC) is an integrated circuit which is manufactured by stacking silicon wafers and interconnecting them vertically using through-silicon vias (TSVs) so that they behave as a single device to achieve performance improvements at reduced power and smaller footprint than two dimensional processes. 3D IC is a simple method of 3D integration schemes that exploit the z-direction to achieve electrical performance benefits. Temperature and reliability are two of the most important challenges associated with 3D ICs. Other challenges include signal integrity and power delivery. Thermal challenges arise from the increased power flux inherent to 3D stacking. TSV-based (Through Silicon Vias) 3D ICs, the approach of monolithic 3D ICs is recently becoming more popular. In this paper, we will discuss various characteristics of TSV that impact on the 3d chip.

Categories and Subject Descriptors:

TSV RC Variation Range, TSV Size, Stress Influence Zone, TSV Re-placement, Device Mobility, Crack Analysis and Optimization for TSV based 3D ICs, Pitch and Angle among TSVs, TSV Placement Style

General Terms: Trans Silicon vias(TSV), Performance

Keywords: 3D chip, power delivery, power supply noise, multi-story

1. Introduction

The integration of large numbers of tiny transistors into a small chip resulted in circuits that are orders of magnitude smaller, cheaper, and faster than those constructed of discrete electronic components.

The increase in number of transistors and scaling down the size of these transistors is based on Moore’s law. Moore's law refers to an observation made by Intel co-founder Gordon Moore in 1965. He noticed that the number of transistors per square inch on integrated circuits had doubled every year since their invention. Moore's law predicts that the number of transistors per square inch has since doubled approximately every 18 months. Unfortunately, the scaling trend accompanied some hardships, which were overcome successfully until now. As the semiconductor devices and metal wires become nano-scaled, the physical limitations in manufacturing and material behaviors pose unprecedentedly great hurdles to semiconductor industry. An approach to this problem is to vertically stack integrated circuits (ICs) or circuitry has emerged as a viable solution for meeting electronic device requirements such as higher performance, increased functionality, lower power consumption, and a smaller footprint. 3D integration of electronic circuits (vs. classical 2D chips) enables tight and efficient coupling of many functional modules within one device Three-dimensional (3D) integration of micro systems and subsystems has become essential to the future of semiconductor technology development. 3D integration requires a greater understanding of several interconnected systems stacked over each other. While this vertical growth profoundly increases the system functionality, it also exponentially increases the design complexity.

With nano-scale interconnect dimensions, the resistivity of wires shoots up, as discussed in the International Technology Roadmap for Semiconductors (ITRS) projection. For short, local nets, the increased resistivity is not a huge problem because the device output resistance dominates the wire resistance. The real problem is on the medium-long nets that connect medium-large design blocks, including intellectual property (IP) blocks. As the devices become smaller and more functionalities are brought onto the chip, the design tends to contain more medium-long nets. The delay of these nets dominates the delay of devices, majorly determining the overall performance of the design. Therefore, reducing interconnect length is crucial to improve overall circuit quality such as timing performance and power consumption.

In this paper, we will see impact of Non-Regular P/G TSV Placement, TSV RC Variation Range, TSV Size, Stress Influence Zone, TSV Re-placement, Device Mobility, Crack Analysis and Optimization for TSV based 3D ICs, Pitch and Angle among TSVs, TSV Placement Style.

2.1 TSV RC Variation Range

TSV RC variation range on the power supply noise show negligible variations from mean values are observed for both static and dynamic noise cases with given RC variation ranges. This is because TSV RC values are much smaller compared with parasitic from 2D P/G grid, decaps, and C4 bumps, hence TSV RC variation does not affect the quality of 3D PDN.

2.2 TSV Size

The increasing TSV size expands footprint area significantly and accommodates more P/G TSVs if we keep the P/G TSV pitch same. Although mean values of both static and dynamic noise change due to TSV size, variation of power supply noise is still negligible.

It is natural that fabrication technology will scale down the TSV size to increase TSV density. However, smaller TSV size might cause more problems in PDN due to increased TSV resistance and its variation.

2.3 Stress Influence Zone

The magnitude of thermo-mechanical stress induced by TSV is highest at the TSV edge. the magnitude of every normal stress component decays fast, and at around $25\mu m$ from the TSV center, stress is almost negligible. For an efficient and fast full-chip stress analysis, it is crucial to confine stress analysis to the manageable extent. Thus, a stress influence zone is defined as a circle with a radius of $25\mu m$ from the TSV center for our baseline TSV with $5\mu m$ diameter. Beyond the stress influence zone, stress induced by the TSV under consideration is neglected.

2.4 TSV Re-placement

Re-placement of TSVs does not effect the circuit.The densely placed TSVs can be repositioned to nearby white spaces if available to reduce the von Mises stress.The von Mises stress is used to predict yielding of materials under any loading condition from results of simple uniaxial tensile tests.

3. Device Mobility

The material property variation on the hole and electron mobility distributions is called device mobility. In semiconductors, the changes in inter-atomic spacing resulting from strain significantly affect the band-gaps, making it easier or harder for electrons—depending on the material and strain—to be raised into the conduction band. This results in a change in resistivity of the semiconductor, which also leads to a change in mobility as follows :

$$\frac{\Delta R}{R} = -\frac{\Delta \mu}{\mu}$$

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$$= [\, \pi'_{11}\sigma_{xx} + \pi'_{12}\,\sigma_{yy}\,]\cos^2\emptyset + [\, \pi'_{11}\sigma_{xx} + \pi'_{12}\,\sigma_{yy}]\,\sin^2\emptyset + \pi_{12}\sigma_{zz} + \pi'_{44}\sigma_{xy}\sin 2\emptyset$$

where σij is the stress in silicon substrate in Cartesian coordinate system, and ϕ is an angle between the wafer orientation and the transistor channel.

4.1 Crack Analysis and Optimization for TSV based 3D ICs:

If there is a small defect such as a void around a TSV, the TSV-induced stress can drive the interfacial cracking between dielectric liner and silicon substrate or the cohesive cracking in dielectric liner and silicon substrate. These cracks may damage transistors nearby, create conducing paths between TSVs (short circuit), and cause the entire chip operation failure in the worst case.

4.2Pitch and Angle among TSVs:

With a fixed victim TSV location, the TSV pitch between a victim and an aggressor is varied from 7.5μm to 60μm. the ERR decreases monotonically as the pitch increases and approaches to the level when there is no aggressor at around 40μm pitch. However, when only one aggressor is considered, the increase of ERR at the minimum pitch compared with the maximum pitch is only 1.4%, which is negligible. The magnitude of ERR decreases when a liner and a landing pad are considered, but the overall ERR trend remains similar.As additional TSVs are introduced, both distance and angle between TSVs become important to the TSV interfacial crack. The stress at a point can be computed by adding individual stress tensors induced by each TSV at this point depending on a relative angle.

4.3 TSV Placement Style

In the irregular TSV placement case, a large variation of ERR values is observed. In addition, many TSVs experience higher ERR values than the regular TSV placement case. This is mainly because TSVs can be placed either densely or sparsely to minimize wirelength in the case of irregular TSV placement scheme. Thus, the ERR of a victim TSV can vary noticeably depending on the placement of nearby aggressor TSVs. Furthermore, since there are regions where group of TSVs are closely placed higher ERR values are observed in the irregular TSV placement style.

5. Die Stacking Technology

There are two possible bonding styles for 3D ICs: face-to-back (F2B) and face-to-face (F2F). In F2B bonding, TSVs are used for inter-die connections. Thus, the number of 3D connections can be limited by the TSV pitch as well as TSV area overhead. The face-to-face (F2F) bonding employing F2F vias is another attractive technology as this does not require additional silicon area for 3D connections. TSV resistance and capacitance values are calculated based. It is assumed that TSV diameter is much larger than F2F via size as manufacturing reliable sub-micron TSVs is challenging. Additionally, the physical size of F2F via can be made comparable to the top metal dimension, around twice the minimum top metal (M9) width in the Synopsys 28nm library.

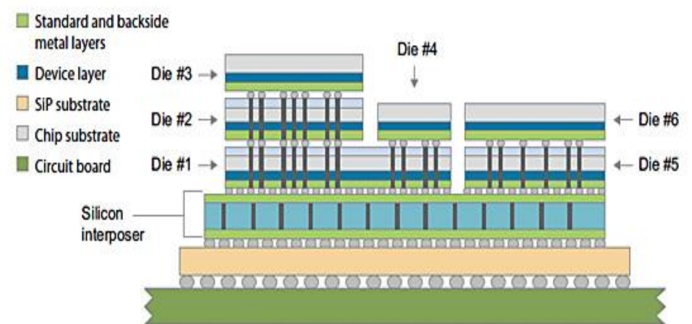

Fig 1: Die bonding styles

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6. CONCLUSION

This paper analyzes on the impact of P/G TSV placement styles and TSV RC variation on the 3D power delivery network,a full-chip TSV thermo-mechanical stress and reliability analysis flow and optimization methods for TSV-based 3D ICs,a chip/package co-analysis of thermo-mechanical stress and reliability as well as mobility and performance variations.

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