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VHDL implementation of logic BIST (Built in self-test) Architecture for high test coverage in VLSI chips.

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Abstract

Very Large Scale Integration (VLSI) has made a dramatic impact on the growth of integrated circuit technology. It has not only reduced the size and the cost but also increased the complexity of the circuits. The positive improvements have resulted in significant performance/cost advantages in VLSI systems. There are, however, potential problems which may retard the effective use and growth of future VLSI technology. Among these is the problem of circuit testing, which becomes increasingly difficult as the scale of integration grows. Because of the high device counts and limited input/output access that characterize VLSI circuits, conventional testing approaches are often ineffective and insufficient for VLSI circuits. The vital role of primitive polynomials for designing PN sequence generators. The standard LFSR (linear feedback shift register) used for pattern generation may give repetitive patterns. Which are in certain cases is not efficient for complete test coverage. The LFSR based on primitive polynomial generates maximum-length PRPG.Built-in self-test (BIST) is a commonly used design technique that allows a circuit to test itself. BIST has gained popularity as an effective solution over circuit test cost, test quality and test reuse problems. In this paper we are presenting an implementation of a tester using VHDL

Keywords: LFSR (linear feedback shift register), PRPG (Pseudo random pattern generator), MISR (Multiple input signature register),.Primitive polynomial, Galois field , BIST (Built in self-test).

1. Introduction

Logic built-in self-test (L-BIST) is a design for testability (DFT) technique in which a portion of a circuit on a chip, board, or system is used to test the digital logic circuit itself. With logic BIST, circuits [1] that generate test patterns and analyze the output responses of the functional circuitry are embedded in the chip or elsewhere on the same board where the chip resides. As the complexity of circuits continues to increase, high fault coverage [3] of several types of fault models becomes more difficult to achieve with traditional testing paradigms. Integrated circuits are presently tested using a number of structured designs for testability (DFT) techniques. In this paper we use the BIST for multiplier technique. And its part LFSR, CUT (multiplier), MISR. In the test mode, a set of test patterns are applied to the circuit and responses are collected. The test responses are then compared with fault-free responses to determine if the CUT (multiplier) works properly.

PROPOSED WORK

In the previous works the test vector generators are based on normal polynomials so the test patterns may repetitive so the test coverage limits. Some fault may not be recognized .but in our proposed work we design the primitive polynomial based on Galois field. For example 4 bit pattern generator should generates 2^4 – 1= (15) test vectors. But there may be possible that 2 or more test vectors generated may be same .because test vector generated randomly. Hence effective no of test vectors are less. if our test vectors are less than our test coverage range shrinks. But in our proposed work our primitive

polynomial based pattern generator generates non-repetitive test vectors. ie. If we use 4 bit PRPG it will generates 15 different test patterns. That means test patterns not repeats. So it will cover a large range of faults.

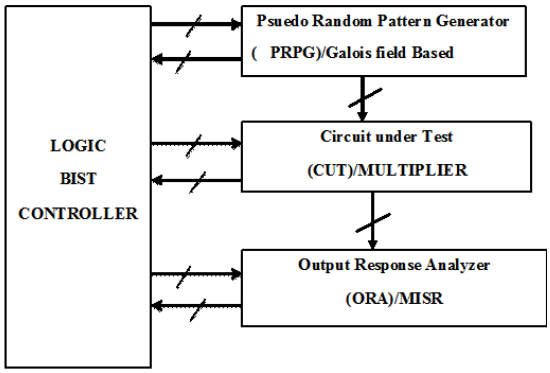

Fig. 1: Proposed LBIST ARCHITECHURE for multiplier for high test coverage

(a) Galois filed based PRPG LFSR(pseudo random pattern generator)

For logic BIST applications, in-circuit PRPG constructed from linear feedback shift registers (LFSRs) are most commonly used to generate test patterns or test sequences for exhaustive testing, pseudo-random testing, and pseudo-exhaustive testing. Exhaustive testing always guarantees 100% single-stuck and multiple-stuck fault coverage. This technique requires all possible 2^n test patterns to be applied to an n-input combinational circuit under test (CUT), which can take too long for combinational circuits where n is huge; therefore, pseudo-random testing is often used for generating a subset of the 2n test patterns and uses fault simulation to calculate the exact fault coverage. In some cases, this might become quite time consuming, if not infeasible. In order to eliminate[2] the need for fault simulation while at the same time maintaining 100% single-stuck fault coverage, we can use pseudo-exhaustive testing [2] to generate 2^wor 2^k-1 test patterns, where w<k<n, when each output of the n-input combinational CUT at most depends on w inputs. For testing delay faults, hazards must also be taken in to consideration.

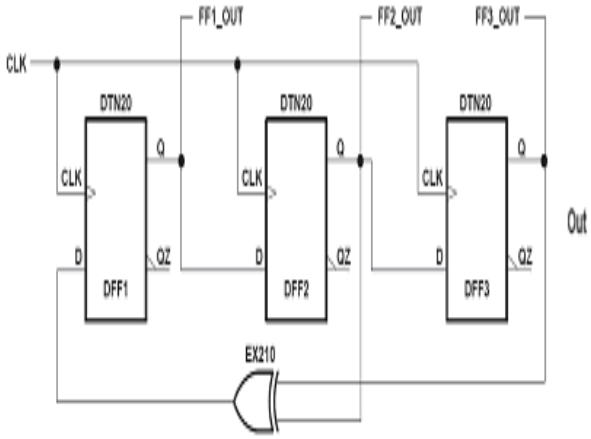

Fig. 2: Linear feedback shift register

(b) CUT (circuit under test)

Exhaustive testing [6] requires applying 2n exhaustive patterns to an n-input combinational circuit under test (CUT). Any binary counter can be used as an exhaustive pattern generator (EPG) for this purpose; however, because the order of generation of the inputs is not important, it may be more efficient to use an autonomous, maximum-length LFSR that can cycle through all states. To do this, it is necessary to modify the LFSR so that the all-zero state is included. A general procedure for constructing modified (maximum-length) LFSRs that include the all-zero state. These modified LFSRs are called complete LFSRs (CFSRs).

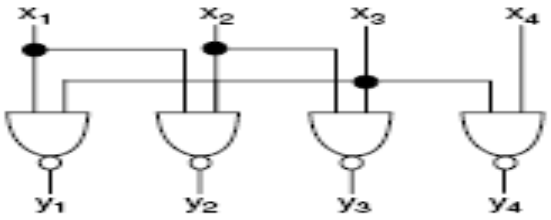

Fig. 3: Circuit Under test

Tests are applied at several steps in the hardware manufacturing flow and, for certain products, may also be used for hardware maintenance in the customer's environment. The tests generally are driven by test programs that execute in Automatic Test [4] Equipment (ATE) or, in the case of system maintenance, inside the assembled system itself. In addition to finding and indicating the presence of defects (i.e., the test fails), tests may be able to log diagnostic information about the nature of the encountered test fails. The diagnostic information can be used to locate the source of the failure.

In other words, the response of vectors (patterns) from a good circuit is compared with the response of vectors(using same patterns) from a DUT(device under test). If the response is the same or matches, the circuit is good. Otherwise, the circuit is faulty.

(c)MISR (Multiple input signature register)

For BIST operations, it is impossible[5] to store all output responses on-chip, on-board, or in-system to perform bit-by-bit comparison. An output response analysis technique must be employed such that output responses can be compacted into a signature and compared with a golden signature for the fault-free circuit either embedded on-chip or stored off-chip.Compaction [2]differs from compression in that compression is loss-less, while compaction is lossy.Compaction is a method for dramatically reducing the number of bits in the original circuit response during testing in which some information is lost. Compression is a method for reducing the number of bits in the original circuit response in which no information is lost, such that the original output sequence can be fully regenerated from the compressed sequence.

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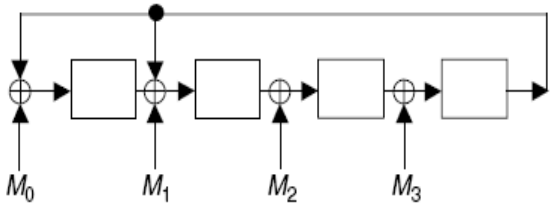

Fig.4: MISR

Response of fault free circuit				
Clock tick	**LFSR O/P**	**O/P of CUT**	**MISR O/P**	**Golden Signature**
1	IIII	0II0	IIII	
2	0III	IIII	II0I	
3	III0	0II0	000I	
4	0I0I	IIII	000I	
5	I0I0	IIII	II00	
6	II0I	0III	0I00	
7	00II	IIII	III0	
8	0II0	0III	00I0	000I
9	II00	IIII	IIII	
10	000I	IIII	I0I0	
11	00I0	0II0	I000	
12	0I00	IIII	II00	
13	I000	0II0	0I00	
14	I00I	IIII	0III	
15	I0II	IIII	000I	

Response of faulty circuit				
Clock tick	LFSR O/P	O/P of CUT	MISR O/P	Signature
1	IIII	0II0	IIII	
2	0III	IIII	I0II	
3	III0	0II0	I0II	
4	0I0I	IIII	00I0	
5	I0I0	IIII	I0I0	
6	II0I	0III	I000	
7	00II	IIII	0I0I	
8	0II0	0III	0I0I	0000
9	II00	IIII	0I0I	
10	000I	IIII	II0I	
11	00I0	0II0	0II0	
12	0I00	IIII	00II	
13	I000	0II0	I00I	
14	I00I	IIII	III0	
15	I0II	IIII	0000	

FAULT TESTING

The BIST pattern generation techniques described above mainly target structural faults, such as stuck-at faults[1] and bridging faults, which can be detected with one pattern vectors. For delay faults requiring two-pattern vectors for testing, these methods do not provide adequate fault coverage. In this section, we discuss a few approaches that can be used for delay fault testing.Unlike structural fault testing that requires an exhaustive one-pattern set of 2^ntest patterns, an exhaustive two-pattern set of $2^n(2^n-1)$patterns is required to test delay faults in an n-input CUT exhaustively. This means that, for delay fault testing, one must use a test pattern generator (TPG) with 2n or more stages. A maximum length LFSR having 2n stages[1] is called a double-length LFSRhas shown that when all even or odd stage outputs (called even taps or odd taps) of a 2n-stage double-length LFSR are connected to the n-input CUT, the LFSR can generate $2^{2n}-1$ vectors to test the CUT exhaustively. While all delay faults are tested exhaustively, there is a potential problem that the test set could cause test invalidation due to hazards present in the design. Test invalidation or hazards can occur when more than one circuit inputs change values. More importantly, a circuit embedded with BIST circuitry can be easily tested after being integrated into a system. Periodic in-system self-test, even using test patterns with less than perfect fault coverage, can diagnose problems down to the level where the BIST circuitry is embedded. This allows system repair to become trivial and economical. Here we have table of finding golden signature.

VHDL IMPLEMENTATION

VHDL implementation of logic BIST (built in self test) Architecture for multiplier circuit for high test coverage in vlsi chips using EDA tool Xilinx's 8.2i, and simulation is done on Modelsim 6.3F. The RTL (register transfer level) of LBIST is shown is below.

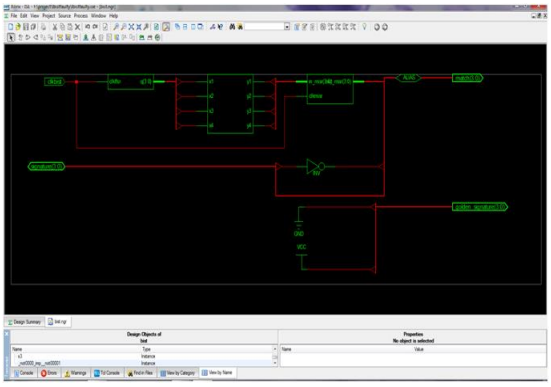

Fig. 5: RTL for LBIST

Register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals. The RTL of logic BIST for multiplier is shown in figure and may be synthesize in Xilinx's FPGA.

SIMULATION RESULTS

The simulation is done on Modelsim and described below. In case of faulty circuit when the test vectors are supplied the product of the inputs gives faulty output. This is clearly verified by the simulation result of faulty circuit.When this faulty circuitcomes under the test, the signature generates (00010) which mismatches from the golden signature (0001) which is already stored.

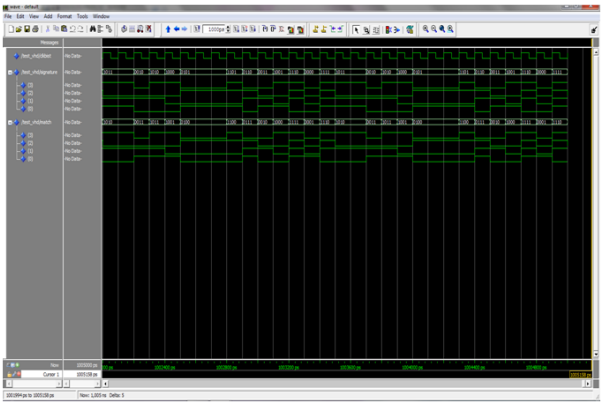

Fig. 6: Simulation Results

CONCLUSION

An implementation of BIST logic using VHDL. LFSR is used as a pseudorandom sequence generator. Signature analysis is used to make verification of the circuit. Signature mismatch with the reference signature means that the circuit is faulty. However there is a small probability that the signature of a bad circuit will be the same as a good circuit. When longer sequence is used signature analysis gives high fault coverage.

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