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DESIGN OF FIR FILTER USING VEDIC MULTIPLIER WITH COMPRESSORS AND PROPOSED CSLA

G.Divya[1], V.Malleswara Rao[2]

[1] PG Scholar, Department of ECE, QIS College of Engineering and Technology, Ongole, India

[2] Assistant Professor, Department of ECE, QIS College of Engineering and Technology, Ongole, India

divya.gorrepati64@gmail.com

Abstract

An adder and a multiplier are main components of an arithmetic unit. An efficient adder and multiplier design, essentially improves the performance of a complex DSP system. Carry Select Adder (CSA) is a fastest adder used in many processors to accomplish fast arithmetic function. Many different adder architecture designs have been developed to increase the efficiency of the adder. It is very commonly known that per second any processor can perform millions of work functions in semiconductor industry. In this paper, we propose a technique for designing of FIR filter using multiplier based on compressor and a proposed carry select adder. Unnecessary logic operations are removed to design an efficient carry select Adder. The proposed FIR filter is simulated and synthesized by using Xilinx ISE.

Keywords: Carry Select Adder (CSA), Vedic multiplier using Compressor, FIR Filter.

I. INTRODUCTION

Area of Digital Signal Processing (DSP) is of extreme importance as it performs the processing of digital signals. A complex DSP system involves several adders and multipliers. An efficient design of adders and multipliers improves the performance of complex signal processing system. Adders and multipliers are the fundamental components which are very frequently found in the many different networks and in different blocks of many systems like controllers and processing chips. A system's performance is basically estimated by the ability of the working of adder and multiplier. In digital adders; addition speed is restricted by the requirement of necessary time for a carry to propagate through the adder. The sum for each bit position in conventional ripple adder is created in sequential manner after the previous bit position has been added and carry transferred into the next position. By reducing the required necessary time to determine carry bits, there is a chance of enhancing the speed in adders. It is possible with Carry Select adder. CSA is used to eliminate the problem of carry propagation delay by separately producing multiple carries and then carry is selected to generate the final sum. However, CSA consumes more area because it uses many pairs of ripple carry adders(RCA) to produce the partial sum and carry by considering Cin = '0' and Cin ='1' respectively, then the final sum and carry are selected by the use of multiplexers .

II. PROPOSED CSLA DESIGN

The proposed CSLA structure is as shown in Fig.5. It is composed of one half-sum generation (HSG) unit, one full sum generation (FSG) unit, one carry-generation (CG) unit, and one carry-selection (CS) unit. The CG unit composed of two units namely CG0 and CG1 corresponding to input-carry '0' and '1', respectively [6]. Input to the HSG unit is two n-bit operands A and B and outputs are half-sum (HS) word S0 and half-carry (HC) word C0 of width n-bit each. CG unit receives both S0 and C0 from HSG unit and gives two n-bit full-carry words c01 and c11, corresponds to carry-input '0' and '1' ,respectively. The carry selection unit selects final carry based on the cin from two anticipated carry words c01 and c11 If cin = 0 then it selects C01; otherwise it selects c11. Cout is the MSB of c obtained from CS unit and remaining (n-l) LSBs of CS unit are XORed with (n-l) MSBs of half-sum (s0) in the FSG unit to obtain final-sum. The proposed logic formulation for the CSLA is given by

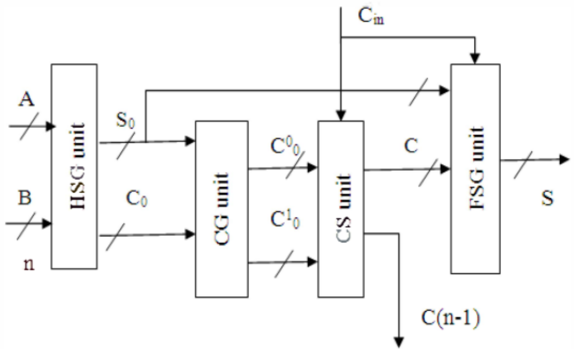


Figure 1: proposed CSLA structure

S_0 (i) = A (i) ^ B (i)
C_0 (i) = A (i). B (i)
$C^0{}_1$ (i) = $c^0{}_1$ (i-1) x s_0 (i) + c_0 (i) for ($c^0{}_1$ (0) = 0)
$C^1{}_1$ (i) = $c^1{}_1$ (i-1) x s_0 (i) + c_0 (i) for ($c^1{}_1$ (0) = 0)
C (i) = $c^0{}_1$ (i)
C (i) = $c^1{}_1$ (i)
C_{out} (i) = c (n - 1)
S (0) = s_0 (0) ^ c_{in}S (i) = s_0 (i) ^ c (i - 1)

III. VEDIC MULTIPLIER WITH COMPRESSORS

Multiplication in most of the signal processing algorithms is a very basic operation. Multipliers generally occupy large area, have high latency and consumes considerable amount of power. Therefore designing of low power multiplier has been an essential part in any system design. In this paper we used modified compressor technique to boost up the speed of operation. So for the purpose of speed multiplication we use innovative technique known as URDHWA multiplier compressor (UMC). Here in this paper we used modified 4:2 compressor and 7:2 compressors for additional purpose in multiplication

To understand the working of 4:2 compressors, we made the basic architecture in figure 2. If we must add four inputs & one carry input bit, then we can do this operation with the help of 4:2 compressors and gives three outputs. The basic design of 4:2 compressor which we have designed with the help of full adder

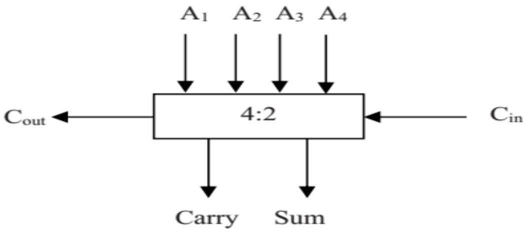


Figure 2: Block Diagram of 4:2 Compressors

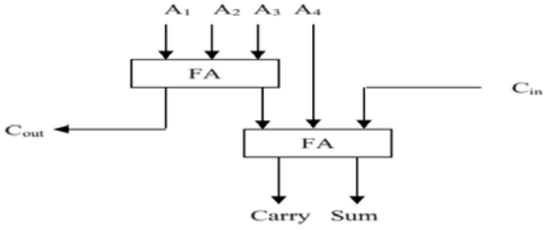


Figure 3: 4:2 Compressors

In the same way, figure 5 shows the 7:2 compressor designs which can add 7 bits of input and 2 carry output from the previous stages, at a time.We have designed 7: 2 compressors with the help of two 4:2 compressors.

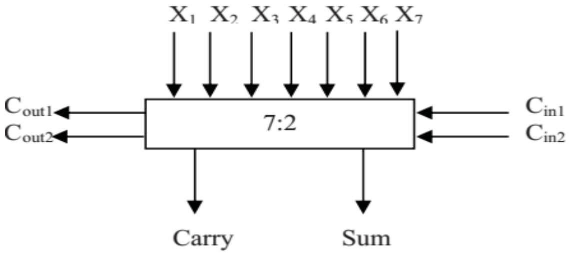


Figure 4: Block Diagram of 7:2 Compressors

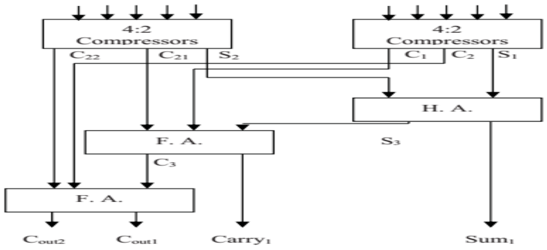


Figure 5: 7:2 Compressors

III. FIR FILTER

We have designed FIR filter using the above proposed CSLA and Vedic Multiplier with compressors. In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time. For a FIR filter of order N, each value of the output sequence is a weighted sum of the most recent input values:

$$Y(n) = \sum_{n=0}^{N-1} h(n)x(n-k)$$

Where, x(n) is the nth input time sequence, h(n) be the filter coefficient and Y(n) represents the nth output filter response sequences.
In Fig6, the block diagram shows the FIR filter design using proposed CSLA and Vedic multiplier with

compressors. This was simulated and tested in Xilinx ISE 9.2.

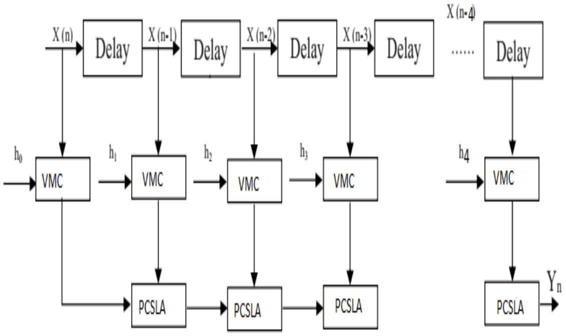


Figure 6: FIR filter using the proposed CSLA and Vedic Multiplier using compressors

IV. SIMULATION RESULTS

In this section, we discuss the efficiency of our proposed CSLA and Vedic Multiplier with compressors. And, we also verify the designed FIR filter using above adder and multiplier.
To study the efficiency of the designed FIR filter, we studied the proposed CSLA efficiency and Vedic Multiplier with compressor efficiency separately using simulations.

Table 1: BEC Square root Vs Proposed CSLA

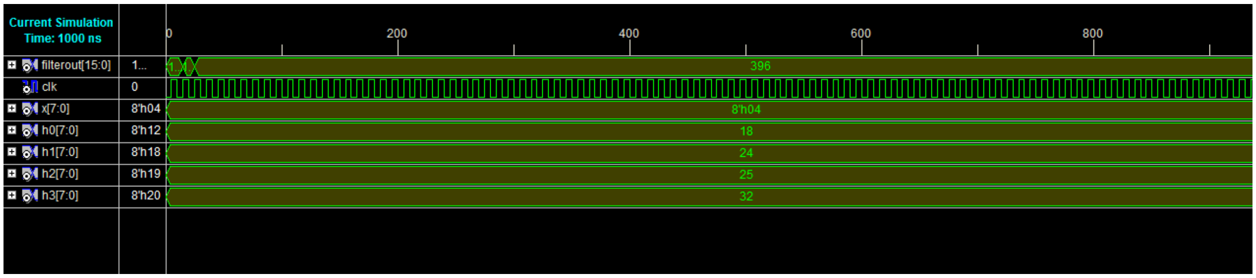
BEC based Square root-CSLA	Proposed CSLA
Area: - Number of slices = 27 out of 4656 Number of 4I/P LUTS = 47 out of 9312	Area: - Number of slices = 22 out of 4656 Number of 4I/P LUTS = 40 out of 9312
Delay – 17.763ns	Delay – 17.507ns
Power – 117mW	Power- 103mW

Table 1 shows comparison between BEC based square root CSLA and the proposed CSLA. In terms Area, Delay and Power the proposed CSLA showed better results compared with BEC CSLA. Hence, the designed CSLA is more efficient compared to conventional CSLA designs available.

Table 2: Array multiplier Vs Vedic multiplier

Array multiplier	Vedic multiplier with compressor
Delay:29.993ns	Delay:26.516ns

From table 2 comparisons, the proposed Vedic multiplier with compressors showed less delay compared to conventional array multiplier from our simulations.
Since both the proposed adder and multiplier are proved efficient than conventional adders and multiplier respectively, the proposed FIR filter with the proposed CSLA and Vedic multiplier with compressor is efficient that conventional FIR filters.
Fig 7 shows the output for the FIR filter designed in Xilinx ISE. It can be seen from the diagram that the FIR filter design using the proposed adder and multiplier is successful.



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filterout[15:0]   1...     396
clk               0
x[7:0]            8'h04    8'h04
h0[7:0]           8'h12    18
h1[7:0]           8'h18    24
h2[7:0]           8'h19    25
h3[7:0]           8'h20    32
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Figure 7: FIR output

V. CONCLUSION

We removed all the unnecessary logic operations present in conventional CSLA and proposed a new logic formulation for CSLA. In the suggested model, the selection of carry (CS) is performed before the calculation of final sum. Carry selection unit can be implemented by using AND-OR gates instead of multiplexer. Since it follows specific bit pattern. we introduce unique compressor technique i.e. Vedic multiplierusing compressor. By using this multiplier and Proposed CSLA. Our proposed FIR filter was simulated and synthesized by using Xilinx ISE design 9.2. As future work, the multiplier and adder performance can be tested within an ALU and compared with several other existing multipliers and adders.

VI.REFERENCES

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Author Details

	Ms.G.Divyahas received B.TECH Degree in electronics & communication engineering from QIS INSTITUTE OF TECHNOLOGY affiliated to university of JNTUK in the year 2013. She is currently pursing M.TECH in VLSI& EMBEDDED SYSTEM from QIS COLLEGE OF ENGINEERING & TECHONOLOGY
	Mr.V.Malleswara Rao, received the B.E Degree from SRKR ENGINEERING COLLEGE, Bhimavaram in 2009 and received the M.TECH degree from R.V.COLLEGE OF ENGINEERING, Bangalore in the year 2012. He has been working as an ASSISTANT PROFESSOR in the department of electronics & communication engineering, QIS COLLEGE OF ENGINEERING & TECHONOLGY, Ongole, A.P since 2012.