

Design and Implementation of High Speed Parallel Micro programmed FIR Filter using Wallace tree and Vedic Multiplier

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Abstract

The micro architecture of digital FIR filter consists of a data path and a control unit. The data path is the computational engine of FIR filter and mainly consists of adders, multipliers and delay elements. The hardware implementation of a Sequential and parallel digital FIR filter architecture using a novel micro programmed controller is presented. The main advantage of the micro programmed controller is its flexibility in modifying the micro program stored in ROM based control memory. To improve the performance of FIR filter, an efficient multiplier is required. Wallace tree and Vedic multipliers are used for the implementation of sequential and parallel micro programmed FIR filter architectures we have proposed a novel high speed and area efficient Vedic multiplier using compressors is used for the implementation of sequential and parallel micro programmed FIR filter architectures. The proposed technique, a 4-tap sequential and parallel FIR filter is implemented using Xilinx Spartan 3e FPGA. The proposed FIR filter is coded in VERILOG. The design can be easily modified to implement higher-order and high speed FIR filters which are commonly used in video and image processing applications.

I. INTRODUCTION

Digital filters are normally used to filter out undesirable parts of the signal or to provide spectral shaping such as equalization in communication channels, signal detection or analysis in radar applications. Adders, multipliers and shift registers are the basic building blocks commonly used in the implementation of digital filters. Different architectures of digital filters can be realized to achieve the same transfer function. The architectures possess different attributes in the form of speed, complexity and power dissipation [1]. Finite impulse response (FIR) and infinite impulse response (IIR) are two such filters used in different applications.

FIR filters are the important building blocks for digital signal, video and image processing applications. Basically, FIR filter performs a convolution on a window of N data samples. A common implementation of the FIR filter is shown in fig. 1, which is also known as direct form FIR filter. As can be seen from the figure, N -tap or $(N-1)$ th order FIR filter consist of N shift registers, N multipliers and N -

1 adders. The impulse response of the FIR filter can be directly inferred from the tap coefficients (W). The multiplier is the fundamental component which decides the overall performance of the FIR filter [2].

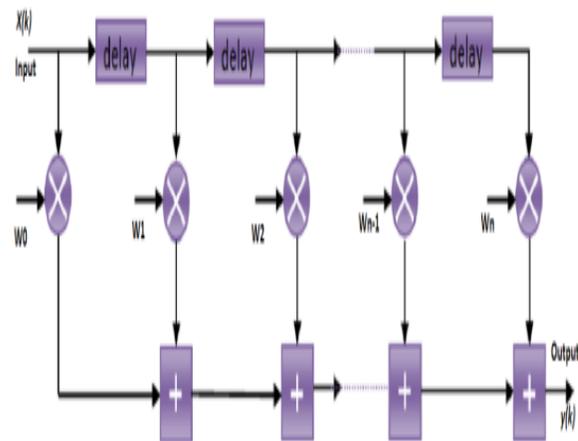


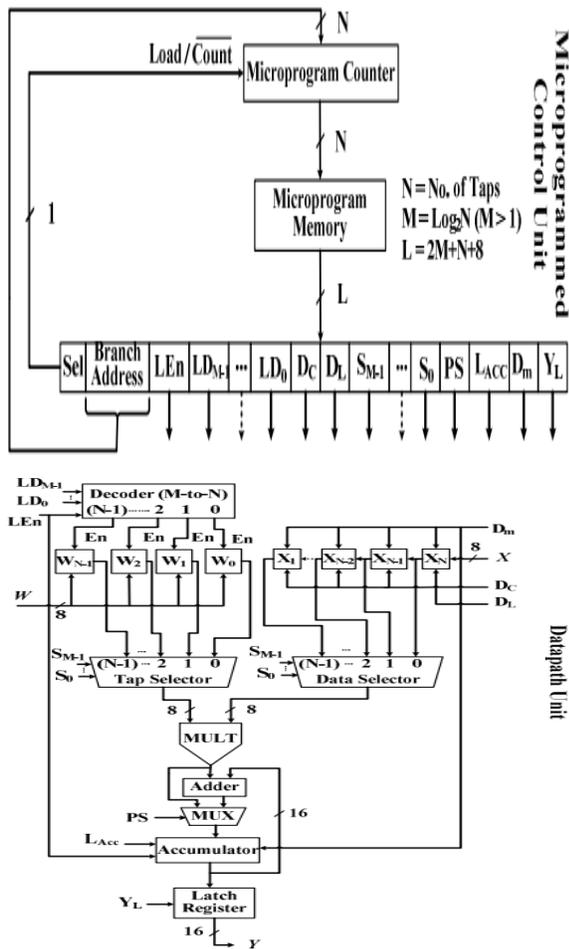
Figure 1: Direct form FIR filter

II. MICRO PROGRAMMED FIR FILTER

The micro programmed FIR filter consists of a data path and a micro program control unit (MCU). The most important advantage of the MCU is its flexibility.

I. Sequential Architecture of Micro programmed FIR Filter

The sequential architecture of N -tap micro programmed FIR filter is shown in Fig. 2. It basically comprises of a MCU and a data path unit. The MCU consists of a microprogram counter and microprogram memory. The data path unit comprises of $2N$ data (X) and coefficient (W) registers and M -to- N decoder ($M = \log_2 N$), two N -input multiplexers for selecting the data and coefficients, a multiplier and an adder, a two input multiplexer to control the flow of data from multiplier or accumulator, one 16-bit accumulator and a 16-bit register to latch the data [8].



Controls signals for data path unit

Figure 2: Architecture of sequential micro programmed FIR filter

II. Parallel Architecture of Micro programmed FIR Filter

The parallel architecture utilizes multiple adders and multipliers, based on the size of the FIR filter, in contrast to single adder and multiplier used in the sequential architecture design. Fig. 3 illustrates the parallel architecture of the micro programmed FIR filter [8]. The data path micro architecture of 4-tap parallel FIR filter consists of the following sub-

modules: Four 8-bit data registers, One 2-to-4 decoder, Four 8-bit coefficient registers, Four multipliers (8×8), Three 16-bit adders, One 16-bit register for latching the output.

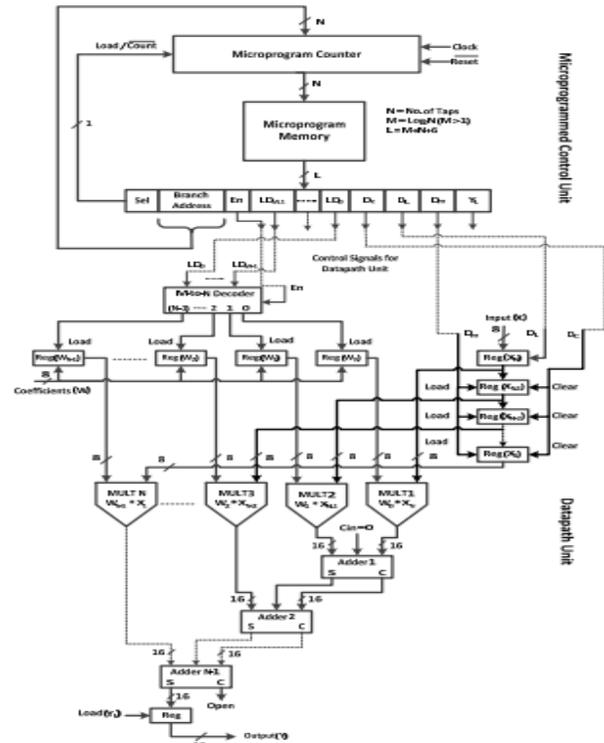


Figure 3: Architecture of parallel micro programmed FIR filter

III. VEDIC MULTIPLIER DESIGN

Vedic mathematics is an ancient form of mathematics which was developed in India by Sri Bharati Krishna Tirthaji, a renowned Sanskrit scholar and mathematician of his times. It is based on sixteen Sutras or algorithms [12]. *Urdhva Tiryakbhyam Sutra* (vertically and crosswise algorithm) is used for efficient digital multiplication. Its calculation is defined by vertical and crosswise product that gives advantage over the normal conventional horizontal multiplication. For binary number, the multiplication operation is reduced to bitwise "AND" operation and the addition operation uses full or half adders.

As mentioned earlier, Vedic Mathematics can be divided into 16 different sutras to perform mathematical calculations. Among these the *Urdhva Tiryakbhyam Sutra* is one of the most highly preferred algorithms for performing multiplication. The algorithm is competent enough to be employed for the multiplication of integers as well as binary numbers. The term "*Urdhva Tiryakbhyam*" originated from 2 Sanskrit words *Urdhwa* and *Tiryakbhyam* which mean "vertically" and "crosswise"

respectively [7]. The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques, is the fact that it utilizes only logical “AND” operations, half adders and full adders to complete the multiplication operation. Also, the partial products required for multiplication are generated in parallel and apriori to the actual addition thus saving a lot of processing time.

The Vedic mathematics concept is applied to develop modular RTL Verilog code for 2x2 multiplier which can be used as a building block to develop 4x4 multiplier. An 8x8 multiplier can be further designed using the 4x4 multiplier and so on.

The 4-bit and 8-bit multipliers used Ripple carry adder for the proposed design. The same Vedic multiplier design is realized using Kogge-Stone adder (KSA). KSA is a parallel prefix form of carry look-ahead adder. It generates the carry signals in $O(\log_2 N)$ time, and is thus widely considered as the fastest adder design possible [13-14].

IV. VEDIC MULTIPLIER USING COMPRESSORS

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The compressor adder used in this paper is a 4:2 compressor adder. A lot of research in the past has been carried out on the same [11]. Similar to its 4:2 compressor counterpart, the 7:2 compressors as shown in Fig. 5, is capable of adding 7 bits of input and 2 carry's from the previous stages, at a time. In our implementation, we have designed a novel 7:2 compressor utilizing two 4:2 compressors, two full adders and one half adder. The multiplier based on Urdhwa method of multiplication requires several full adders and half adders to add the necessary partial products. This in turn leads to a large propagation delay due to the reasons explained in the previous section. As part of our novel approach, we combined the compressor architectures explained earlier and utilized the same in the Urdhwa based architecture which was formerly. The architecture for the same has been shown below in Fig.7.

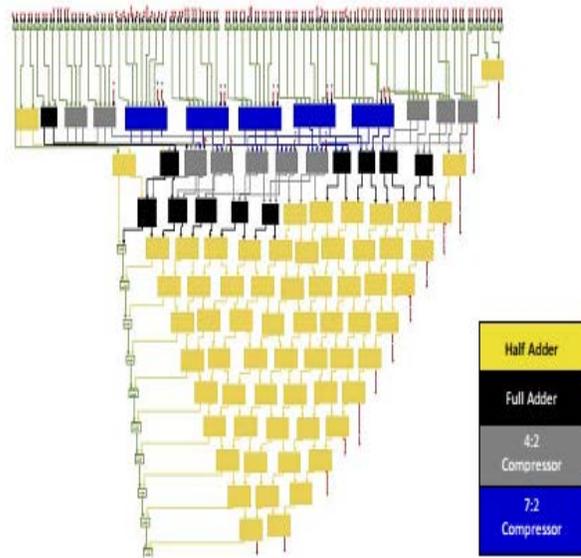


Figure7: Hardware architecture of Compressor based Urdhwa Multiplier

It can be clearly seen from Fig. 7 that the compressor based Urdhwa multiplier requires only 12 parallel stages as opposed to 15 which was in the case of the conventional Urdhwa Tiryakbhyam multiplier. This is a major improvement with respect to high speed multiplier design. Also, it can be seen that, many of the stages have now been reduced to a mere logical XOR operation, with an initiative to reduce area.

V. Simulation Results

I. Sequential FIR Filter



Figure 8.1: Control signals for Sequential FIR Filter

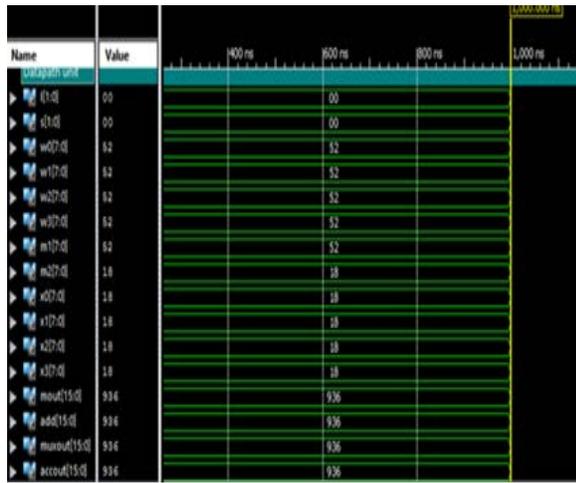


Figure 8.2: Data path unit of Sequential FIR Filter

II. Parallel FIR Filter



Figure 9.1: Control signals for Parallel FIR FilterFig

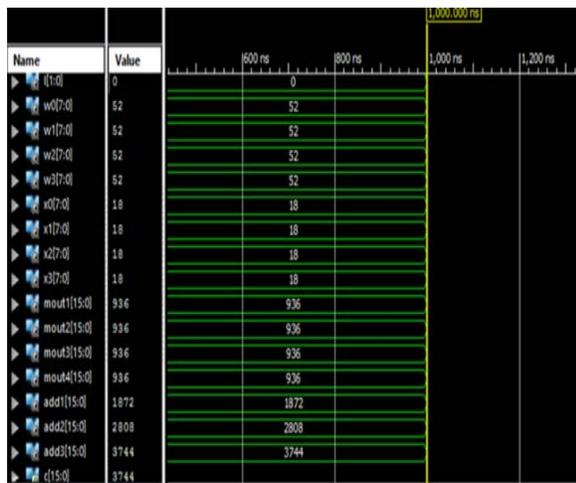
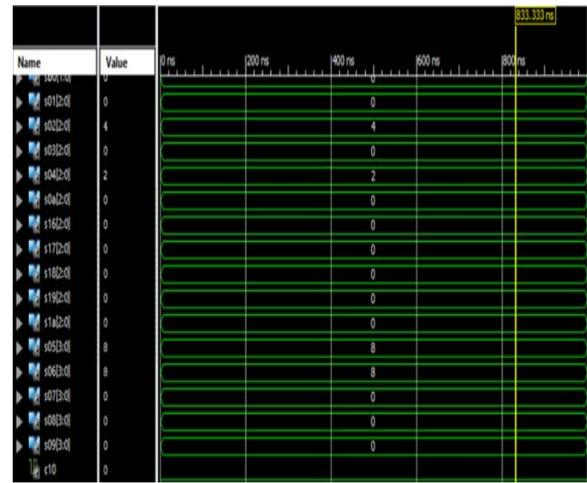
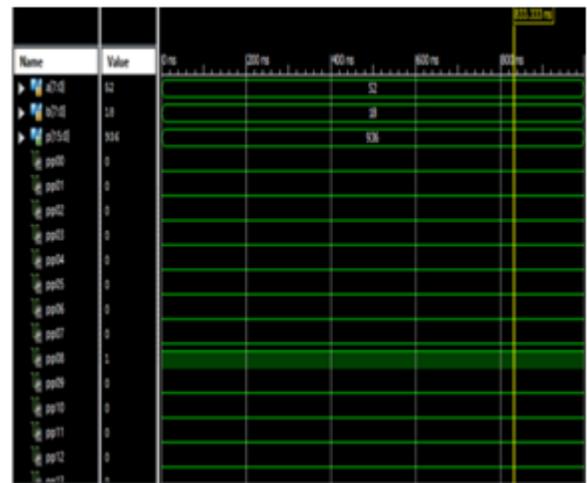


Figure 9.2: Data path unit for Parallel FIR Filter

III.Vedic multiplier using Compressor adders



(a)



(b)

Figure 10: Vedic multiplier using Compressor adders

VI.CONCLUSION

Digital filters are one of the main elements of DSP. FIR filter which mainly comprises of multiply-accumulate structure is the most commonly used digital filter. Since the performance of FIR Filter mostly depends on the multiplier used, an enhanced and improved multiplier will ameliorate the overall system performance. In this paper, we designed and implemented micro programmed sequential and parallel FIR filter architectures in Xilinx spartan3E FPGA using Vedic multiplier/ripple carry adder, Vedic multiplier/Kogge-Stone adder and Vedic multiplier using compressors combinations respectively.

VII.REFERENCES

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