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DESIGN AND IMPLEMENTATION OF SEQUENTIAL AND PARALLEL MICROPROGRAMMED FIR FILTER

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Abstract

The micro architecture of digital FIR filter consists of a data path and a control unit. The data path is the computational engine of FIR filter and mainly consists of adders, multipliers and delay elements. The hardware implementation of a Sequential and parallel digital FIR filter architecture using a novel micro programmed controller is presented. The main advantage of the micro programmed controller is its flexibility in modifying the micro program stored in ROM based control memory. To improve the performance of FIR filter, an efficient multiplier is required. Vedic multipliers are used for the implementation of sequential and parallel micro programmed FIR filter architectures we have proposed a novel high speed and area efficient Vedic multiplier using compressors is used for the implementation of sequential and parallel micro programmed FIR filter architectures. The proposed technique, a 4-tap sequential and parallel FIR filter is implemented using Xilinx Spartan 3e FPGA. The proposed FIR filter is coded in VHDL. The design can be easily modified to implement higher-order and high speed FIR filters which are commonly used in video and image processing applications.

Introduction

Digital filters are normally used to filter out undesirable parts of the signal or to provide spectral shaping such as equalization in communication channels, signal detection or analysis in radar applications. Adders, multipliers and shift registers are the basic building blocks commonly used in the implementation of digital filters. Different architectures of digital filters can be realized to achieve the same transfer function. The architectures possess different attributes in the form of speed, complexity and power dissipation [1] [4].Finite impulse response (FIR) and infinite impulse response (IIR) are two such filters used in different applications. FIR filters are the important building blocks for digital signal, video and image processing applications. Basically, FIR filter [3] performs a convolution on a window of *N* data samples. A common implementation of the FIR filter is shown in fig. 1, which is also known as direct form FIR filter. As can be seen from the figure, *N*-tap or (*N*-1)th order FIR filter consist of *N* shift registers, *N* multipliers and *N*-1 adders. The impulse response of the FIR filter can be directly inferred from the tap coefficients (*W*).The multiplier is the fundamental component which decides the overall performance of the FIR filter [2].

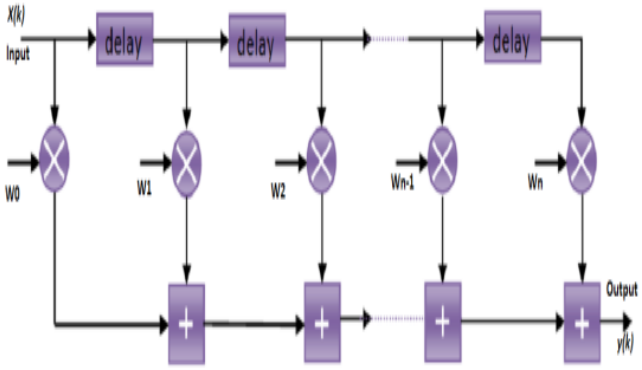

Fig 1: Direct form FIR filter

II. MICRO PROGRAMMED FIR FILTER

The micro programmed FIR filter [5] [7] consists of a data path and a micro program control unit (MCU). The most important advantage of the MCU is its flexibility.

1. Sequential Architecture of Micro programmed FIR Filter

The sequential architecture of *N*-tap micro programmed FIR filter is shown in Fig. 2. It basically

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comprises of a MCU and a data path unit. The MCU consists of a microprogram counter and microprogram memory. The data path unit comprises of 2*N* data (X) and coefficient (W) registers and *M*-to-*N* decoder (*M* = *log2N*), two *N*-input multiplexers for selecting the data and coefficients, a multiplier and an adder, a two input multiplexer to control the flow of data from multiplier or accumulator, one 16-bit accumulator and a 16-bit register to latch the data [8].

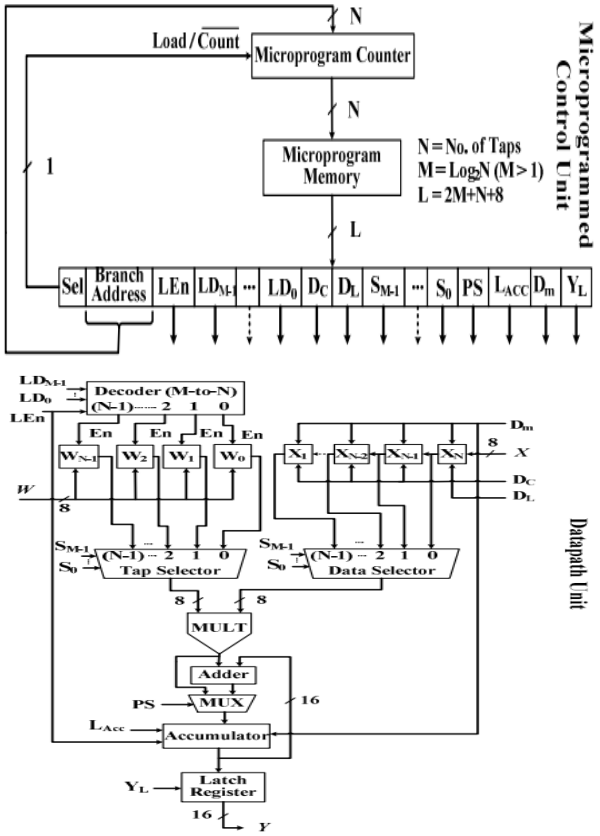


Fig 2: Architecture of sequential micro programmed FIR filter

2. Parallel Architecture of Micro programmed FIR Filter

The parallel architecture [6] utilizes multiple adders and multipliers, based on the size of the FIR filter, in contrast to single adder and multiplier used in the sequential architecture design. Fig. 3 illustrates the parallel architecture of then micro programmed FIR filter [8]. The data path micro architecture of 4-tap parallel FIR filter consists of the following sub-modules: Four 8-bit data registers, One 2-to-4 decoder, Four 8-bit coefficient registers, Four multipliers (8×8),Three 16-bit adders, One 16-bit register for latching the output.

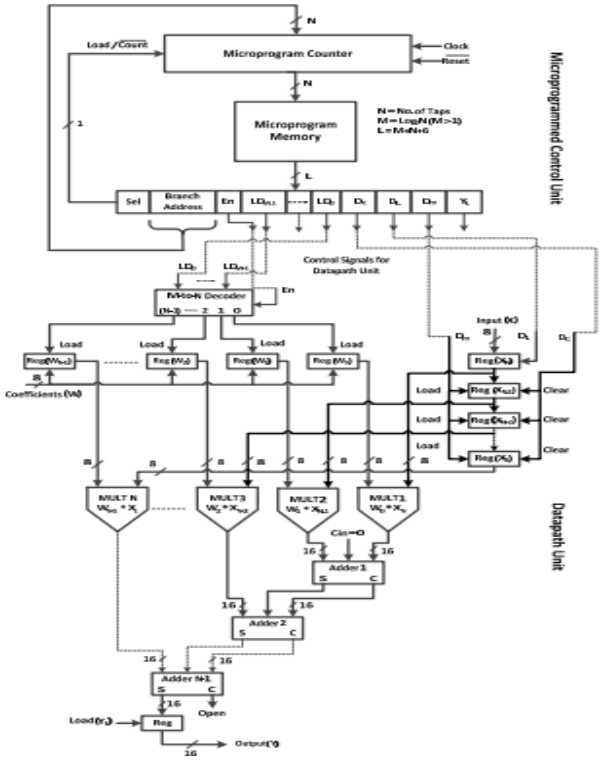
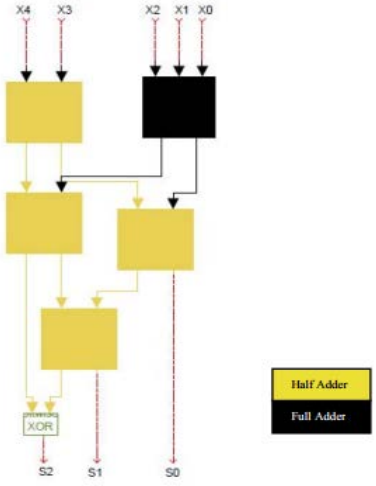


Fig 3: Architecture of parallel micro programmed FIR filter

III. VEDIC MULTIPLIER USING COMPRESSORS

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The compressor adder used in this project is a 4:2 compressor adder. A lot of research in the past has been carried out on the same.



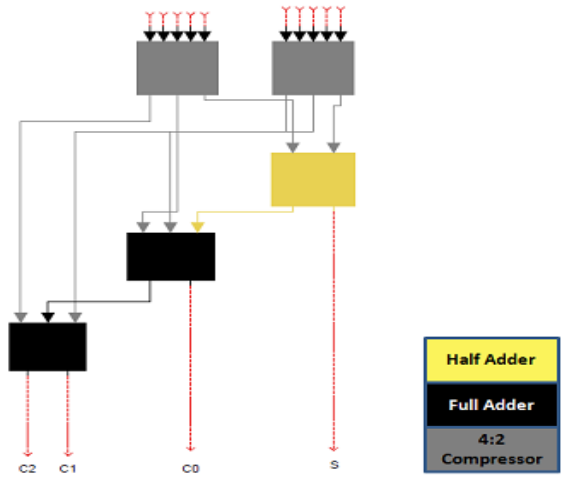


Fig 4: 4:2 Compressor using full adders and half adders

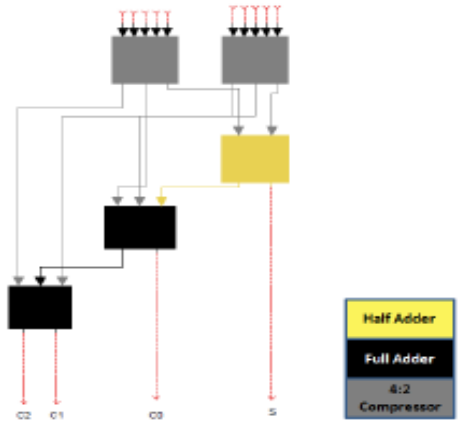


Fig 5: 7:2 Compressor using 4:2 Compressors

Similar to its 4:2 compressor counterpart, the 7:2 compressors as shown in Fig. 5, is capable of adding 7 bits of input and 2 carry's from the previous stages, at a time. In our implementation, we have designed a novel 7:2 compressor utilizing two 4:2 compressors, two full adders and one half adder. The multiplier [9] [10] based on Urdhwa method of multiplication requires several full adders and half adders to add the necessary partial products. This in turn leads to a large propagation delay due to the reasons explained in the previous section. As part of our novel approach, we combined the compressor architectures explained earlier and utilized the same in the Urdhwa based architecture which was formerly. The architecture for the same has been shown below in Fig.6.

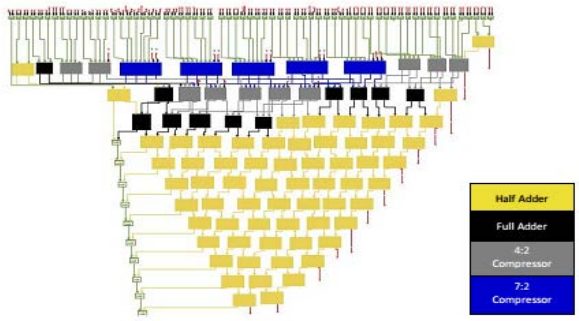


Fig. 6 Hardware architecture of Compressor based Urdhwa Multiplier

It can be clearly seen from Fig. 7 that the compressor based Urdhwa multiplier requires only 12 parallel stages as opposed to 15 which was in the case of the conventional Urdhwa Tiryakbhyam multiplier. This is a major improvement with respect to high speed multiplier design. Also, it can be seen that, many of the stages have now been reduced to a mere logical XOR operation, with an initiative to reduce area.

IV. Simulation Results

Sequential FIR Filter

Fig.7.1 Control signals for Sequential FIR Filter

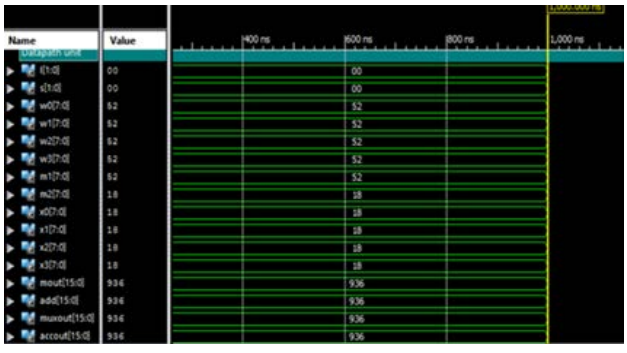


Fig.7.2 Data path unit of Sequential FIR Filter

Parallel FIR Filter

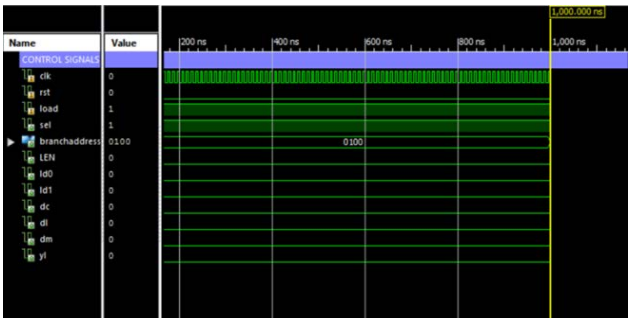


Fig 8.1 Control signals for Parallel FIR Filter

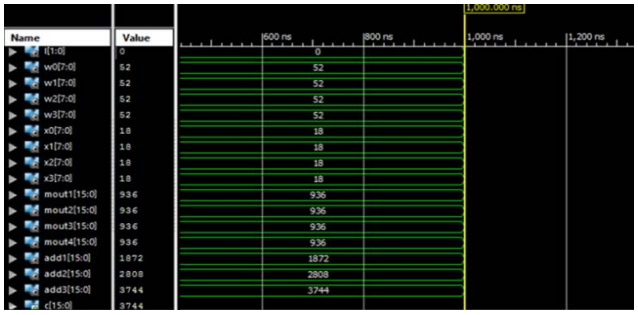


Fig 8.2 Data path unit for Parallel FIR Filter

V.CONCLUSION

Digital filters are one of the main elements of DSP. FIR filter which mainly comprises of multiply-accumulate structure is the most commonly used digital filter. Since the performance of FIR Filter mostly depends on the multiplier used, an enhanced and improved multiplier will ameliorate the overall system performance. In this paper, we designed and implemented micro programmed sequential and parallel FIR filter architectures in Xilinx spartan3e FPGA using Vedic multiplier/Kogge-Stone adder and Vedic multiplier using compressors combinations respectively.

VI.REFERENCES

1. S. M. Qasim, M. S. BenSaleh and A. M. Obeid, "Efficient FPGA implementation of microprogram control unit based FIR filter using Xilinx and Synopsys tools," *Proc. of Synopsys Users Group Conference (SNUG)*, Silicon Valley, USA, pp. 1-14, March 2012.
2. M. A. Ashour and H. I. Saleh, "An FPGA implementation guide for some different types of serial-parallel multiplier structures," *Microelectronics J.*, Vol. 31, PP. 161-168, 2000.
3. S. M. Qasim, A. A. Telba and A. Y. AlMazroo, "FPGA design and implementation of matrix multiplier architectures for image and signal processing applications," *Int. J. Comp. Sci. Network Security*, Vol. 10, No. 2, pp. 168-176, Feb. 2010.
4. M. Obeid, S. M. Qasim, M. S. BenSaleh, Z. Marrakchi, H. Mehrez, H. Ghariani and M. Abid, "Flexible reconfigurable architecture for DSP applications," *Proc. of 27th IEEE Intl. System-on-Chip Conf. (SOCC),* pp. 204-209, Sept. 2014.
5. S. M. Qasim, M. S. BenSaleh, M. Bahaidarah, H. AlObaisi, T. AlSharif, M. Alzahrani and H. AlOnazi, "Design and FPGA implementation of sequential digital FIR filter using microprogrammed controller," *Proc. of 4th Intl. Congress on Ultra Modern Telecommunications and Control Systems and Workshops (ICUMT),* pp. 1002-1005, Oct. 2012.
6. M. S. BenSaleh, S. M. Qasim, M. Bahaidarah, H. AlObaisi, T. AlSharif, M. Alzahrani and H. AlOnazi, "Field programmable gate array realization of microprogrammed controller based parallel digital FIR filter architecture," *Proc. of World Congress on Engineering and Computer Science (WCECS)*, pp 828–831, Oct. 2012.
7. S. M. Qasim and M. S. BenSaleh, "Hardware implementation of microprogrammed controller based digital FIR filter," *IAENG Trans. Engg. Tech.*, Vol. 247, pp 29-40, 2014.
8. M. S. BenSaleh, S. M. Qasim, A. A. AlJuffri and A. M. Obeid, "Scalable design of microprogrammed digital FIR filter for sensor processing subsystem," *IEICE Electronic Express*, Vol. 11, No. 14, pp.1-7, Aug. 2014.
9. W. J. Townsend, E. E. Swartzlander and J. A. Abraham, "A comparison of Dadda and Wallace multiplier delays," *Proc. SPIE*, Vol. 5205, 2003.
10. A. Aljuffri. M. M. AlNahdi, A. A. Hemaid, O. A. AlShaalan, M. S. BenSaleh, A. M. Obeid and S. M. Qasim, "ASIC realization and performance evaluation of scalable microprogrammed FIR filters using Wallace tree and Vedic multipliers," *Proc. of 15th IEEE Intl. Conf. on Environmental and Electrical Engineering (EEEIC)*, pp.1-4, June 2015, Accepted.