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Quad-Fault Tolerant Architecture Design for Ripple Carry Adder

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Abstract

We consider quad fault cases and show how a system can reconfigure from an error causing four faults at maximum. A system must be fault tolerant to decrease the failure rate and increase the reliability of it. Multiple faults can affect a system simultaneously and there is a trade-off between area overhead and number of faults tolerated. Fault tolerant architecture design for a ripple carry adder assuming quad faults.

Keywords: fault tolerant, Ripple carry adder, Test pattern generation.

I. Introduction

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of (or one or more faults within) some of its components. If its operating quality decreases at all, the decrease is proportional to the severity of the failure, as compared to a naively designed system in which even a small failure can cause total breakdown. Fault tolerance is particularly sought after in high-availability or systems. A fault-tolerant design enables a system to continue its intended operation, possibly at a reduced level, rather than failing completely, when some part of the system fails. The term is most commonly used to describe computer systems designed to continue more or less fully operational with, perhaps, a reduction in throughput or an increase in response in the event of some partial failure. That is, the system as a whole is not stopped due to problems either in the hardware or the software. An example in another field is a motor vehicle designed so it will continue to be drivable if one of the tires is punctured. A structure is able to retain its integrity in the presence of damage due to causes such as fatigue, corrosion, manufacturing flaws, or impact. Within the scope of an individual system, fault tolerance can be achieved by anticipating exceptional conditions and building the system to cope with them, and, in general, aiming for self-stabilization so that the system converges towards an error-free state. However, if the consequences of a system failure are catastrophic, or the cost of making it sufficiently reliable is very high, a better solution may be to use some form of duplication. In any case, if the consequence of a system failure is so catastrophic, the system must be able to use reversion to fall back to a safe mode.

II. Quad-Fault Tolerant Architecture

Adder is absolutely essential block in any digital architecture. Among different types of adders ripple carry adder (RCA) is most popular in different type of computing machines because it is simple in structure and easy to implement. It has also high throughput for bit level pipelining. We have taken a 4-bit RCA to make itself reconfigurable. We will also discuss how the same approach can be applied to any system, which can be divided into some identical modules, to make the system fault tolerant. The fault tolerant designs are also cascadable to increase the number of input bits Making a system module wise self-reconfigurable is more cost effective and hardware efficient rather than trying to make the whole system fault tolerant at a time. We will also elaborate how the approach to design a self reconfigurable 4-bit RCA can be applied to design any fault tolerant module. RCA composed of several full adder (FA) cells can be completely tested by a minimum test set of size eight independent of the number of cells in the RCA under Quad-faulty cell assumption. But there is no provision to detect and eliminate the error. Their work cannot take care of bridging faults. We have modified the circuitry to make each intermediate FA controllable and observable to improve the testability. The size of

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eight is minimum since eight test vectors are necessary to exhaustively test just one cell. A simple four bit adder module with its all data inputs and outputs. For checking stuck-at-faults at any of the input or output, only six test patterns suffice. A Simple 4-bit Adder But instead of error at any of the input or output lines, one of the FAs may be faulty itself; i.e., there may be some stuck open or bridging faults or so inside the FA or some transistors in that FA may be faulty. The test Patterns for stuck-at-faults only do not consider these cases. To check for such cases, each FA should be tested exhaustively. All 4 FAs are tested exhaustively to check for any fault in it. Even the same pattern can be replicated to test any x-bit adder (x = any positive integer) and only eight test patterns will suffice for all such cases.

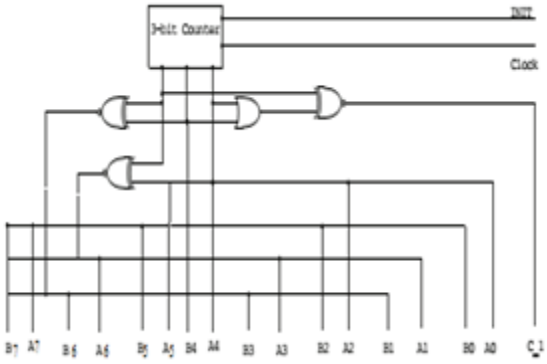


Fig.1. test pattern generator

So, to make the Adder structure fault tolerant, we shall test each FA with all possible input patterns and check whether we get the desired output or not. If not, the Adder block must be faulty! Now, instead of replacing the faulty 4 bit adder completely, we will use the Dynamic Recovery concept to make the adder module fault tolerant itself. Here we will use four spare FA's and if any of the working FA is found to be faulty, then the spare one will start working bypassing the faulty one so that the system can work properly. Four redundant FA's are used along with the four operating FAs to incorporate dynamic recovery feature in the system. If any one of the first four FAs is found to be faulty or its input or output is at some faults, then the system will bypass the inputs and outputs of the corresponding faulty FA to the next FA and the spare four will be activated automatically. To use same carry input to all the FAs, we select the multiplexers (mux) select input CSi as '1'. But if carry input to this FA is at some stuck-at-fault, it will be propagated to the carry input of the next FA giving an overall erroneous output! It now seems that a large number of test vectors are required to test each FA exhaustively as we cannot control the carry inputs of the intermediate FAs due to their direct dependence on output carry of the immediately preceding FAs.

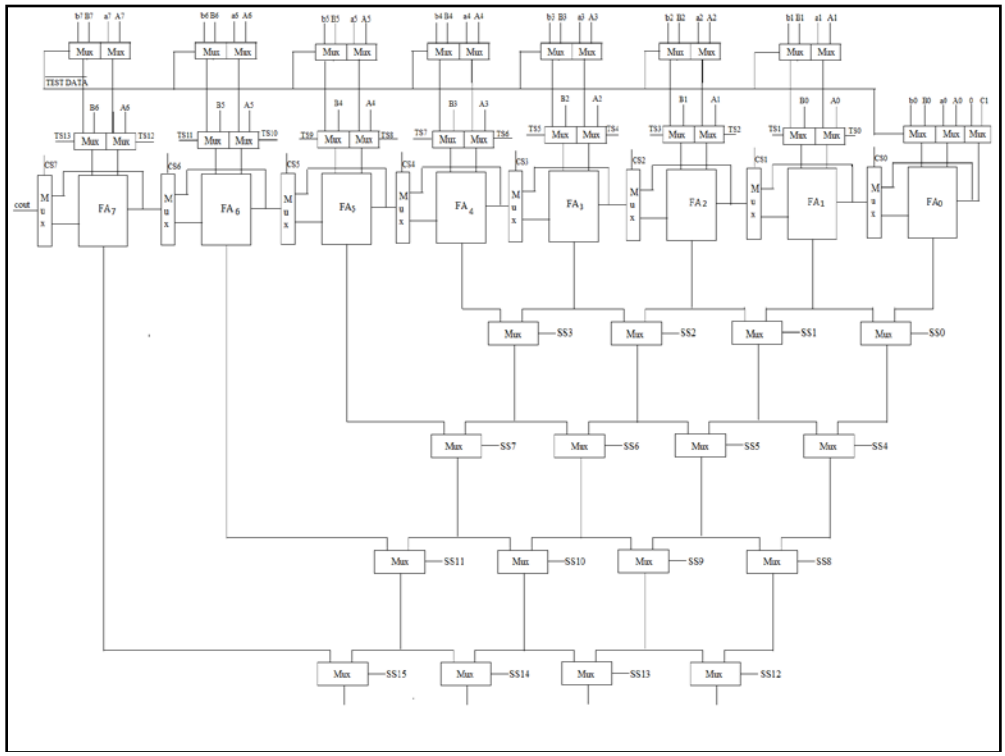
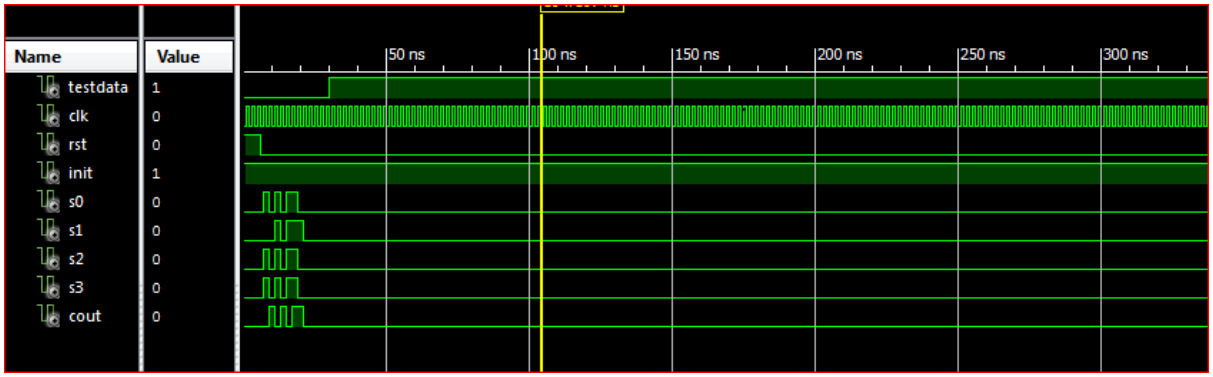


Fig.2.quad-fault architecture

III. SIMULATION WAVEFORMS



IV. CONCLUSION

We have designed a self-reconfigurable fault tolerant 4-bit RCA. A simple four bit Adder module with its all data inputs and outputs. For checking stuck-at-faults at any of the input or output. A Simple 4-bit Adder But instead of error at any of the input or output lines, one of the FAs may be faulty itself; i.e., there may be some stuck open or bridging faults or so inside the FA or some transistors in that FA may be faulty. The test Patterns for stuck-at-faults only do not consider these cases. To check for such cases, each FA should be tested exhaustively. All 4 FAs are tested exhaustively to check for any fault in it. Fault tolerant architecture design for a ripple carry adder assuming quad faults. Digital blocks fault tolerant and these designs can be used in different digital architectures to increase the reliability of the whole system.

V. REFERENCES

1. Y Sato, S. Kajihara, Y. Miura, T.Yoneda, S. Ohtake, I Inoue, H.Fujiwara, "circuit failure prediction mechanism (DART) for high field reliability," IEEE 8th International Conference on ASICON '09, pp. 581-584, Oct. 2009.
2. B. A. Prasad, and F. G. Gray, "Multiple fault detection in arrays of combinational cells," IEEE Transactionson Computers, vol. 100, no. 8, pp. 794-802, 1975.
3. Francisco J. O. Dias, "Truth-table verification of an iterative logic array." IEEE Transactions on Computers, vol. 100, no. 6, pp. 605-613,1976.
4. S.-K. Lu, J.-C. Wang and C.-W. Wu, "C-testable design techniques for iterative logic arrays," IEEE Transaction on VLSI Systems, vol. 3, no. 1,pp. 146–152, Mar. 1995,.
5. W.-T. Cheng and J. H. Patel, "A minimum test set for multiple fault detection in ripple carry adders," IEEE Transaction on Computers, vol. 36, no.7, pp. 891-895, July 1987,.
6. Mukherjee; A. S. Dhar, "Design of a Self-Reconfigurable Adder for Fault-Tolerant VLSI Architecture," 2012 International Symposium on Electronic System Design (ISED), pp. 92-96, Dec. 2012,.
7. J. Sklansky, "Conditional-sum addition logic," IRE Transactions on Electronic Computers, vol. 2, pp. 226-231, 1960.
8. A. Mukherjee, A. S. Dhar, "Design of a Fault-Tolerant Conditional Sum Adder", H. Rahaman et al. (Eds.): VDAT 2012, Springer LNCS 7373, pp. 217–222, 2012

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