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Design of radix 2 and radix4 multipliers with BIST

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Abstract

In VLSI Industry testing is an essential process for making the assurance functionality of the chip. This paper is focusing on one of the test methodology called built-in-self-test (BIST).To introduce a novel test pattern generator (TPG) called Johnson counter for test the modules of the chip.TPG is generated here with the re-configurable Johnson counter and a LFSR generated seed values. Bit EX-OR operation is performed between the re-configurable Johnson counter and the seed. The proposed gray counter TPG was produced using Gray counter and Decoder. The Area and power optimization is achieved. Bist using radix2 multiplier with Gary tpg. We are extended Bist using radix4 multiplier with Gary tpg is coded using VERILOG HDL and simulations, synthesis were performed with Xilinx 13.2 tool.

Keywords: Built-in-self-test (BIST), Test Pattern Generator (TPG), Linear feedback shift registers (LFSR).

1. Introduction

Testing plays a crucial role in any kind of production. The occurrence of imperfection in VLSI circuits results in testing every chip. The possibility of defect might be caused due to various constrains such as malfunctioning of equipments, design errors and material defect. Testing can be performed externally or internally. External testing is performed using automatic test equipment (ATE). The test vectors are generated using ATE and are applied to circuit under test (CUT).The results are analyzed using CAD tools. The drawback of performing testing using ATE is longer time required for testing and high cost of the equipment. Hence there is a shift from external testing to internal testing. Internal testing is performed with the help of built in self test (BIST). BIST reduces difficulty and complexity in testing the circuits. The test vectors generated are applied to the digital circuit and the circuit response obtained is compared with the true response to determine the fault. For the purpose of pattern generation exhaustive testing or Pseudo exhaustive testing or Pseudorandom testing can be performed. Exhaustive testing applies all possible input combination to the digital circuit. The advantage of generating test patterns using exhaustive testing is 100% fault coverage. But the drawback is the increased test time. In Pseudo exhaustive testing the circuits are partitioned into small slices and individual slices are tested using exhaustive testing. In Pseudorandom testing the patterns were generated in random fashion. The produced patterns may or may not be repeatable. The Pseudorandom patterns are generated to reduce the test length thereby reducing the time for testing .In traditional techniques the testing vectors were produced using linear feedback shift register .

II.TPG using Reconfigurable Johnson counter and LFSR

Test Pattern Generator contains the three operational blocks for generating the TPG. Those are

1. Reconfigurable Johnson counter
2. Seed generation using LFSR
3. Bit EXOR operation
4. MISR

Re-configurable Johnson counter

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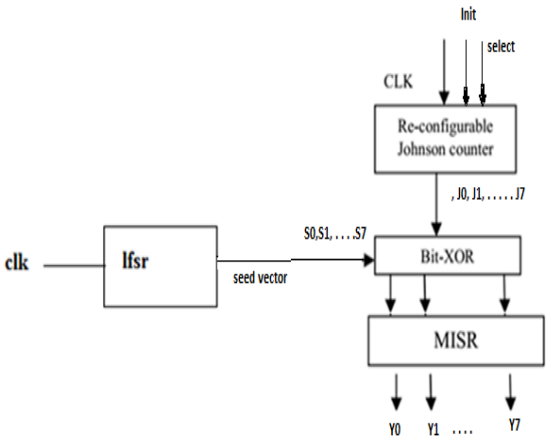

Fig 1 TPG using reconfigarable jhonson counter

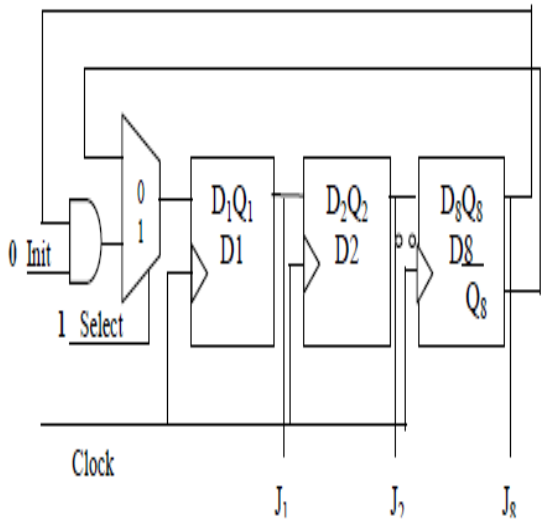

Fig 2 Intialization mode

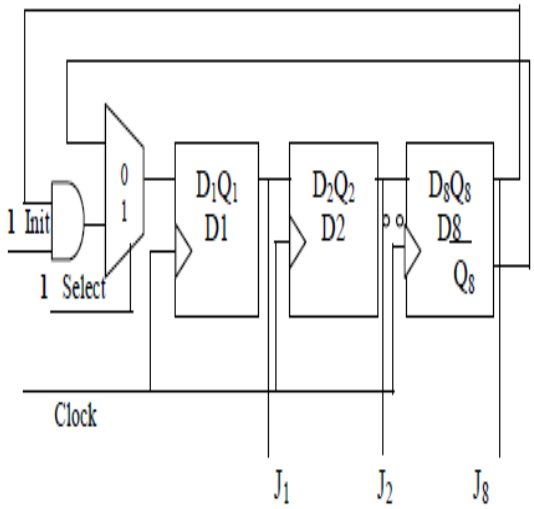

Fig 3 Circular shift mode

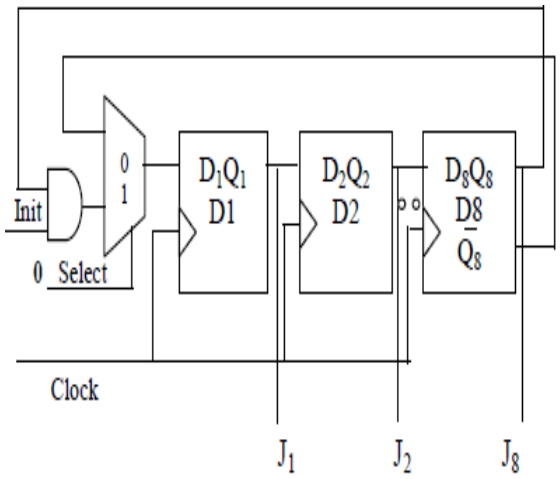

Fig 4 Normal mode

The Johnson vectors were produced by utilizing reconfigurable Johnson counter .reconfigurable Johnson counter is constructed with the help of an AND gate, Multiplexer and eight Delay flip-flops are connected together to store the bits. Johnson vector were made to operate Initialization mode, Circular shift mode and normal mode to initialize the flip flops the select input of the multiplexer assigned with the value 1 and one of the inputs to the and gate is assigned with the value 0 the clock signal is applied to initialize the registers. The initialization operation of the Reconfigurable Johnson counter. The circular shift mode performs shifting operation and the output q8 of d8 register is feedback. To perform circular shift operation the select input of the multiplexer is choosen to be1 and input to the AND gate init is assigned with the value 1 the clock input is clocked to operate Johnson counter in circular mode

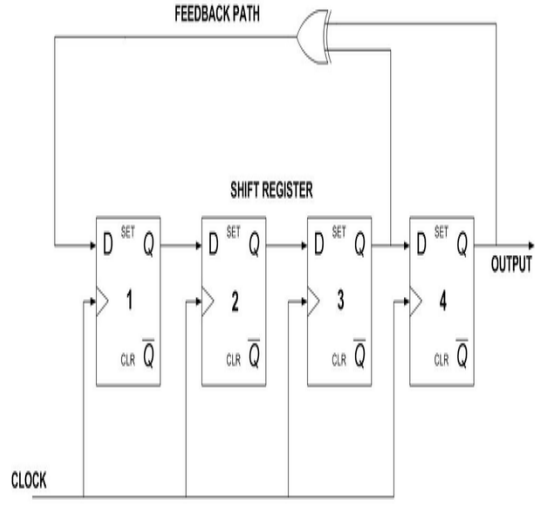

Fig 5 Seed generation using LFSR

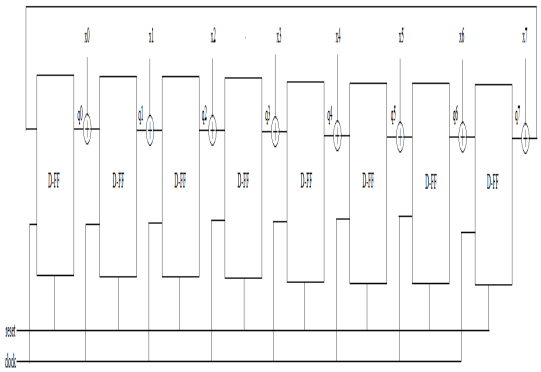

fig 6 MISR

III.TPG using gray counter

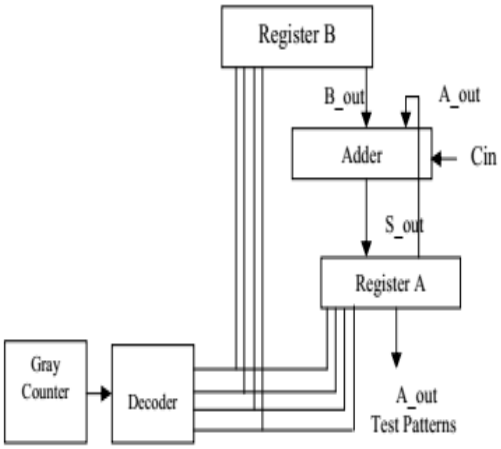

Fig 7 TPG using gray counter

The demand for the portable devices is increasing tremendously. So Area and Power optimization are essential to satisfy the demands of the consumer. The patterns generated using Existing methodology finds complexity in Area and Power. For the purpose of optimization the patterns were generated using Gray code counter. The purpose of choosing gray code counter is to reduce the power requirements. The gray code counters prevent the unwanted signal transition at the input. The input bits vary in single bit position. For every rising edge of the clock four bit gray code results were applied to 3 to 8 Decoder circuit. The results of decoder circuit were applied to the adder circuit through Register B. The set reset flip flop is used as Register A to store the computed result. The patterns were obtained through register A. The patterns produced were tested on Multiplier circuit. The response obtained is compared with the forecasted result to verify the exact functioning of the circuit.

IV. Radix 2&radix4 multiplier with multiplexers

Radix2

Here, we have this recoding unit using multiplexers. Select lines to multiplexer are input bit sequence of multiplier and outputs are according to modified table given in table. So, in this scheme, partial products are always one bit more than input vector. If our multiplier is of n bit then partial products are always n+1.

MODIFIED BOOTH'S RECODING TABLE FOR RADIX 2

X_i	X_{i-1}	Y	Partial Product Explanation
0	0	0	All 0's
0	1	1.A	$[A_{(n-1)}, A]$
1	0	-1.A	$[A_{(n-1)}, (-A)]$
1	1	0	All 0's

Table 1 radix 2 table

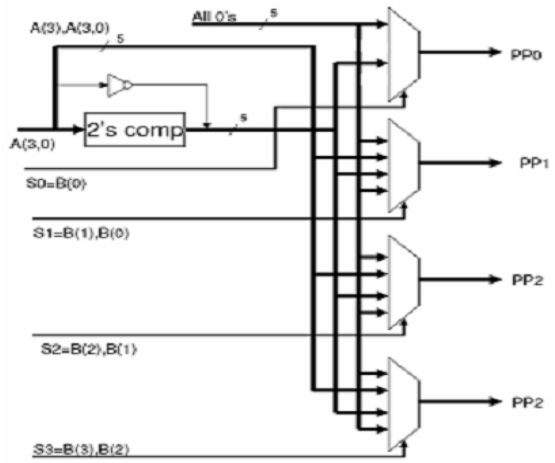

Fig 8. Architecture of radix 2

In this architecture, select lines for multiplexers are multiplier input bits taken according to recoding scheme given in table. Which are similar to General Booth's recoding scheme. We have used 4 multiplexer out of which 3 are 4x1 and one is 2x1.Each input vector is of n+1 of input bits of multiplier. 0^{th} and3rd input vector are always zero and 1stposition input vector is multiplier input (A) appended with extra zero at MSB to increase its

width to n+1, it does not change original value. 2nd position input vector is taken 2's complement of input (A) with appending inverted MSB bit of input vector. This architecture generates four partial products vector according to table vector. This architecture generates four partial products vector according to table.

Radix4

This is also same scheme as explained above that reduces partial products so it is very helpful for fast multiplication of long input bit sequences. But, here partial product which we got from recoding unit is always 2 bit more than input bits. If our inputs are of n bit then partial products are n+2 bit. Recoding scheme is shown in table, and architecture of this recoding unit is shown in fig. In this radix scheme, select lines of multiplexers are 3 bits but first multiplexer can be of 2 select lines, which are two LSBs and remaining multiplexers have 3 input select lines

Table 1 radix 4 table

MODIFIED BOOTH'S RECODING UNIT FOR RADIX 4

X_{i+1}	X_i	X_{i-1}	Y	Partial Product Explanation
0	0	0	0	All 0's
0	0	1	1.A	$[A_{(n)}, A_{(n)}, A]$
0	1	0	1.A	$[A_{(n)}, A_{(n)}, A]$
0	1	1	2.A	$[A_{(n)}, A, 0]$
1	0	0	-2.A	$[\overline{A_{(n-1)}}, -A, 0]$
1	0	1	-1.A	$[\overline{A_{(n-1)}}, \overline{A_{(n-1)}}, -A]$
1	1	0	-1.A	$[\overline{A_{(n-1)}}, \overline{A_{(n-1)}}, -A]$
1	1	1	0	All 0's

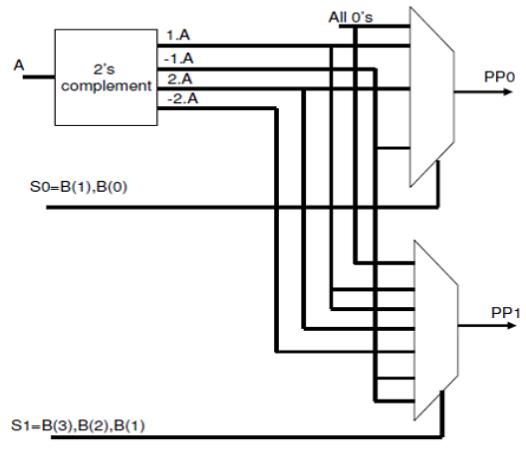

Fig 9. Architecture of radix 2

The architecture of Booth's radix 4 recoding schemeis same as explained in section A shown in fig. Only difference is partial products are n+2 in width of input vector according to table. Now, all these partial products need to be added properly to get correct output. So, we designed modified partial product adder unit (array of adders) which moreover similar to Brown's array

Partial Product Adder

The partial product obtained form Booth's recoding unit needs to be added properly to get correct output of a multiplication. The addition scheme of partial product is same as Browns array multiplier except for MSBs. MSBs of partial products need to be added carefully. For that, new structure of an adder array is proposed. This modification removes the problem of large number of correction bits, which in turn require more number of adders. The proposed partial product adder arrays for 4 bit input sequence using radix 2 algorithms.

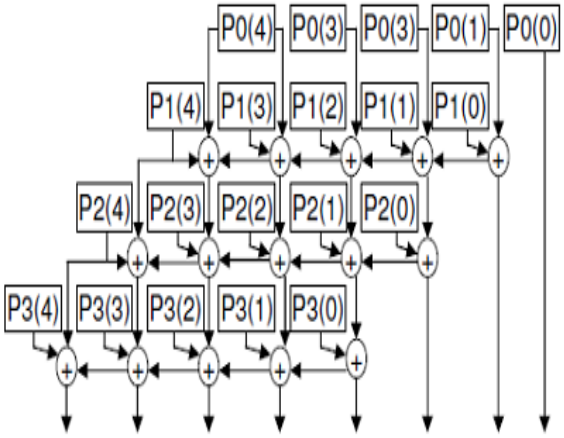

Fig 10. Radix 2 of 4 bit input

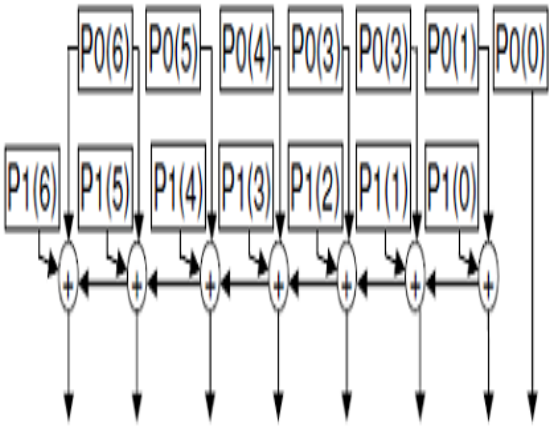

Fig 11. Radix 4 of 4 bit input

V. SIMULATION WAVEFORMS

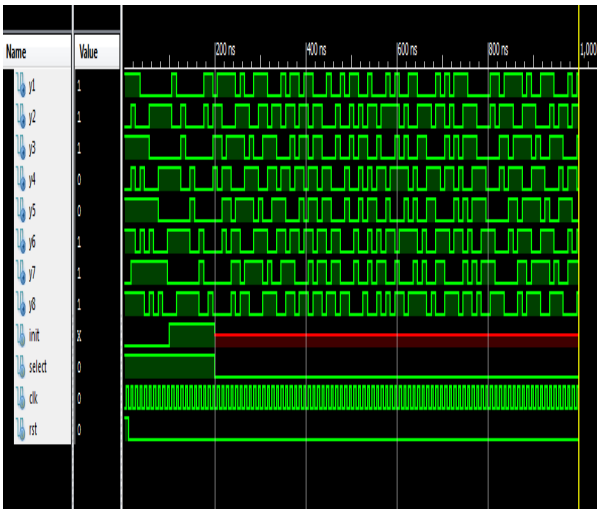

Fig 12 Johnson Counter TPG

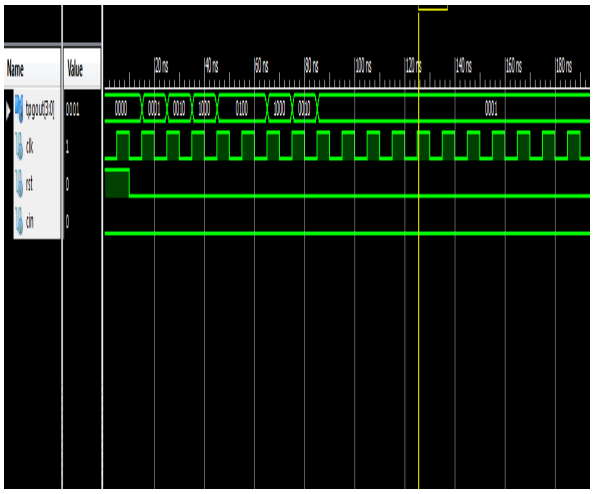

Fig 13 Gray Counter TPG

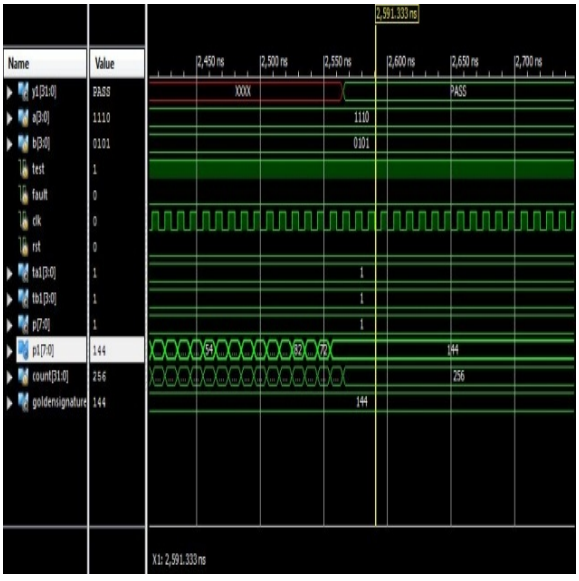

Fig 14 Testing of Multiplier Using TPG

VI. CONCLUSION

The architecture has been proposed to generate the test patterns for BIST. Power and area optimization is achieved by generating patterns using gray counter TPG. Bist using radix2 multiplier with Gary TPG. We are extended Bist using radix4 multiplier with Gary TPG is coded using VERILOG HDL and simulations, synthesis were performed with Xilinx 13.2 tool.

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