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DESIGN OF EFFICIENT RECONFIGURABLE INTERPOLATION FILTER

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Abstract

An Interpolation filter with filter length, N=16 and up-sampling factors 2, 4 and 8 is developed in this paper. The Vector Generation Unit and Arithmetic Unit, which are the major blocks of the proposed architecture is developed by writing Verilog code. Another block Coefficient Selection Unit is developed using multiplexer-based design. A novel block-formulation is presented to share the partial results for parallel computation of filter outputs of different up-sampling factors. In this architecture, the partial results are made to reuse in the Arithmetic unit of the proposed method by which computational complexity reduces. Further, the filter length is increased to 32 and similar analysis is done by using up-sampling factors 2, 4, 8 and 16. Unlike the existing methods, all the blocks are developed using single software. All synthesis and simulation reports are observed using Xilinx 14.2 ISE.

KEYWORDS: Arithmetic unit, Interpolation filter, vector generation unit, up-sampling factor.

1. Introduction

Interpolation filter is an anti-imaging filter which is used to suppress the undesired Interference effect resulting due to up-sampling the baseband signal [1]. Generally, pulse shaping filters are used as interpolation filters because of its high ISI rejection ratio and high bandwidth limitation criteria. An up-sampler together with an interpolation filter is called Interpolator. The function of an up-sampler is to change the sampling rate of base band signal. The interpolation filter consists of different coefficient vectors for different up-sampling factors of baseband signal [2].

SDR is a technology that enables for digital implementation of wide band trans-receivers of multi-standard wireless communication [3]. A multi-standard SDR system involves interpolators with different filter coefficients, filter lengths and up-sampling factors to meet the frequency specifications. For example, consider UMTS which is the acronym for Universal Mobile Telecommunication Standard. It uses interpolators with interpolation factors (4, 8 and 16) and filter lengths (25, 49 and 47) respectively. A SDR receiver uses huge amount of resource when these interpolators are implemented individually in a hardwired circuit. A reconfigurable FIR Interpolation filter is the most desirable filter for are source and power constrained multi-standard SDR receiver which would support various up-sampling factors as well as filter specifications.

For the past few years, many multiplier and multiplier-less designs have been developed for efficient hardware realization of reconfigurable FIR filters and filter-banks for SDR channelization [4]- [9]. A few multiplier-less designs are proposed for interpolation filter [10]-[13]. Symmetric property of PSF and LUT decomposition methods are used in [10] to reduce the area complexity of 1:4 interpolation filters. In [11], further the in-phase and quadrature-phase filters are used with which LUT words are saved. As a result, it offers a significant saving of area complexity of interpolation filter. But the disadvantage is that both the designs in [10] and [11] cannot be reconfigured for up-sampling factor other than 4. To overcome this disadvantage, distributed arithmetic (DA) based reconfigurable architecture is proposed in [12]. In this existing method, the disadvantage is that their proposed structure

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requires large size DA-LUT which is not at all favourable for single chip realization. In [13], similar design of [12] is proposed with the use of LUT-less DA technique by which the area complexity can be reduced. It involves less area than previous proposed methods and supports base band signal of low sampling rates.

Consider an interpolation filter with up-sampling factor P and filter length N which involves an input matrix of size (P x M), where M= N/P. Input matrix of interpolation filter varies for different filter lengths and up-sampling factors. As a result, the reconfigurable interpolation filter has irregular data-flow which makes hardware realization difficult. This problem is solved to some extent by assuming a constant filter length which is equal to the length of the largest size filter. Whereas the smaller filter is realized using the same structure using zero padding. With this assumption, the input matrix changes only when up-sampling factor P is varied. The key contributions of this paper are:

- A novel block formulation is presented for efficient realization of reconfigurable interpolation filter.
- Partial results can be re-used in reconfigurable interpolation filter.

The rest of the paper is organized as follows: implemented architecture is discussed in section II. Simulation results are illustrated in section III. Conclusion is discussed in section IV.

II. IMPLEMENTED ARCHITECTURE

The implemented architecture is shown in figures 1 and 2 with filter lengths N=16 and 32 respectively. It consists of three blocks. They are: (i) Coefficient Selection Unit (CSU),(ii) Arithmetic Unit (AU) and (iii) Vector Generation Unit (VGU). Here Arithmetic Unit and Vector Generation Unit are the major blocks of the architecture. The final output is taken at Arithmetic Unit block, which will be the blocks of Interpolation filters with up-sampling factors 2, 4 and 8 for filter length 16 and for filter length 32, an extra block with up-sampling factor 16, is obtained at the output. In this architecture, the partial results can be reused for parallel computation of filter outputs of various up-sampling factors p_1=2, p_2=4, p_3=8 and p_4=16 for filter length, N=32 and up-sampling factors p_1=2, p_2=4 and p_3=8 for filter length, N= 16. It does not require any reconfiguration to compute filter outputs of a particular interpolation filter with different up-sampling factors.

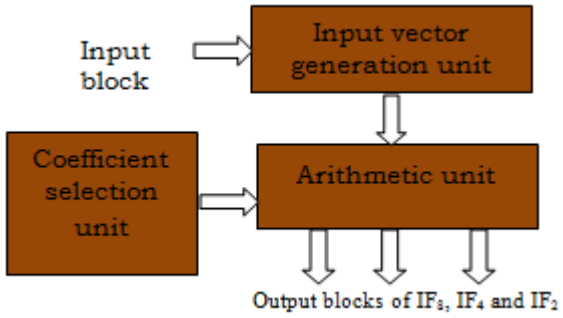

Figure 1: Reconfigurable architecture with filter length, N=16

The Coefficient Selection Unit, CSU is comprised of N number of J : 1 multiplexers or N number of ROM LUTs of depth J words each, where N is the filter length and J is the number of interpolation filters of different coefficient vector to be realized in the reconfigurable architecture. To avoid longer critical path delay, multiplexer-based CSU is used for J $\leq$ 4, otherwise the ROM-based CSU is preferred. The required coefficient-vector of a particular interpolation filter is selected in one cycle from the CSU.

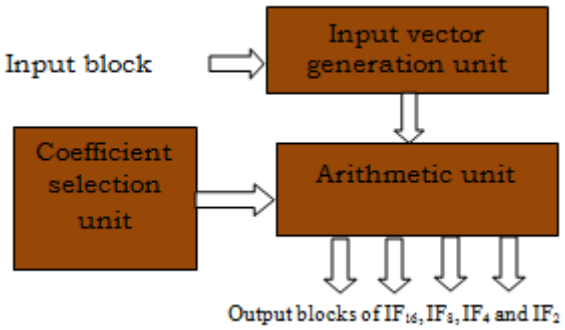

Figure 2: Reconfigurable architecture with filter length, N=32

The structure of Arithmetic Unit for a set of up-sampling factors p_1=2, p_2=4, p_3=8 for filter length 16 is shown in figure 3. For filter length 32, the Arithmetic Unit is shown in figure 4. It has up-sampling factors 2, 4, 8 and 16. Here the outputs of Interpolation filter with up-sampling factor 16, IF_{16} are added separately to obtain the filter outputs of Interpolation filter with up-sampling factor 8, IF_8. In the same way, the outputs of Interpolation filter with up-sampling factor 8, IF_8 are further added to obtain the filter outputs of Interpolation filter with up-sampling factor 4, IF_4 and the method is same for obtaining filter output for up-

sampling factor 2 as well. In developing Arithmetic Unit block, we require N/p_1 multiplier units and (N/p_1 - 1) adder units, where p_1 =2, which is the lowest up-sampling factor and N =16 and 32, which are the filter lengths of the architecture. Therefore, we require 8 multiplier units and 7 adder units for filter length, N=16. For filter length, N=32, 16 multiplier units and 15 adder units are required. In Arithmetic Unit, one of the inputs is taken from Coefficient Selection Unit and another input is taken from the Vector Generation Unit. The output obtained at the Arithmetic Unit will be the blocks of Interpolation filters with different up-sampling factors.

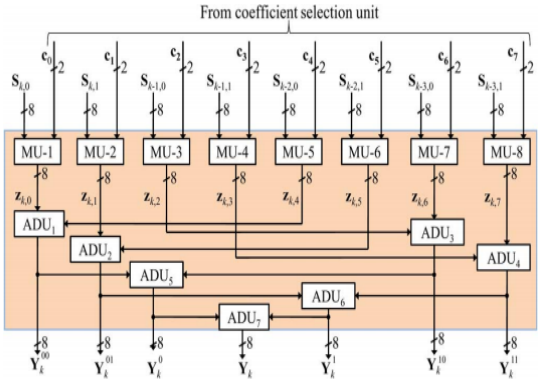

Figure 3: Internal Structure of Arithmetic Unit (AU) for filter length, N=16

It is always better to realize the architecture for lowest up-sampling factor, i.e. for Interpolation filter with up-sampling factor 2, IF_2. Further filter outputs of higher up-sampling factors of a given set can be obtained in parallel without performing any extra computation i.e. Interpolation filters with up-sampling factors 4, 8 and 16.

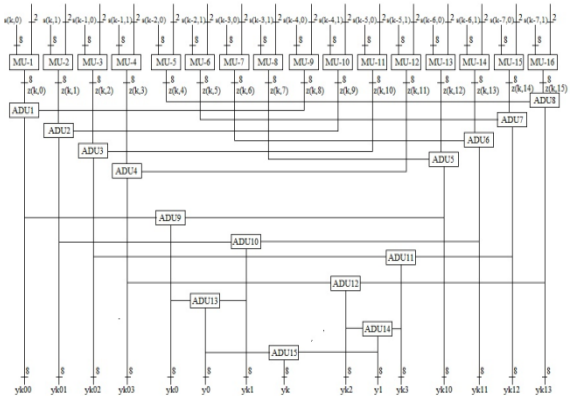

Figure4. Internal Structure of Arithmetic Unit (AU) for filter length, N=32

The figure 5 illustrates the Vector Generation Unit, VGU with filter length, N=16 and lowest up-sampling factor p_1=2. We require N-1 registers and N/p_1 data vectors to develop this block.

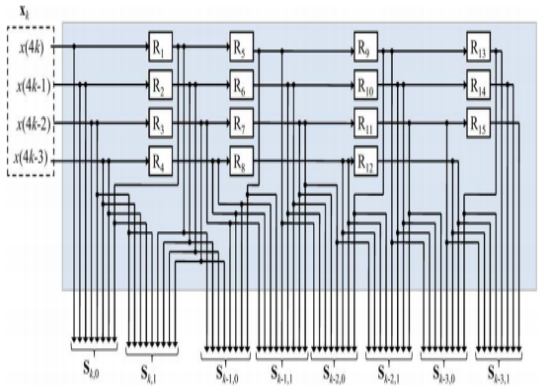

Figure 5: Internal structure of Vector Generation Unit for filter length, N=16

The figure 6 shows the internal structure of Vector Generation Unit, VGU with lowest up-sampling factor, p_1=2 and filter length, N=32. A Vector Generation Unit is developed using N-1 registers as already mentioned. If filter length, N=32, we require 31 registers to develop Vector Generation Unit. It receives a block of input samples in every cycle and produces N/p_1 data vectors. For filter length, N=32, we get 16 data vectors. Similarly, if filter length, N=16, we require 15 registers and 8 data vectors to develop the Vector Generation Unit.

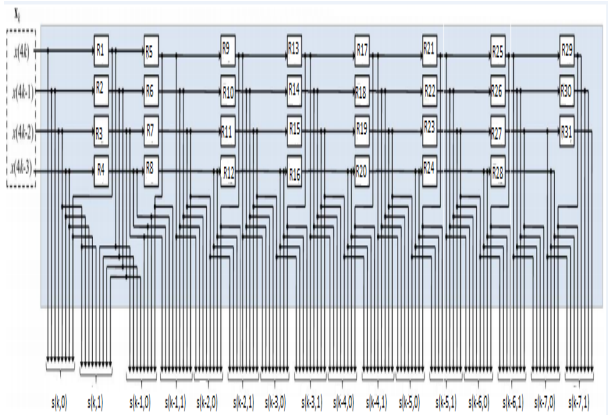

Figure 6: Internal structure of Vector Generation Unit for filter length, N=32

The complexity of Vector Generation Unit is independent of input block size unlike Arithmetic Unit whose complexity increases proportionately with block size.The overall complexity of the architecture is independent of up-sampling factors.

III. RESULTS

The figure 7 illustrates the final stage output of the architecture for filter length, N=16. The inputs will be taken from Coefficient Selection Unit and Vector Generation Unit. Both these inputs will be given to an Arithmetic Unit. The output is taken at Arithmetic unit with output as blocks of interpolation filters with up-sampling factors 2, 4 and 8 represented by IF_2, IF_4 and IF_8 respectively.

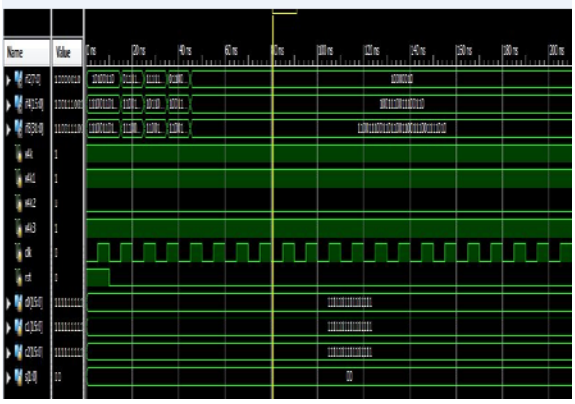

Figure 7: Final stage output for filter length, N=16

The figure 8 illustrates the final stage output of the architecture for filter length, N=32. The inputs will be taken from Coefficient Selection Unit and Vector Generation Unit. Both these inputs will be given to an Arithmetic Unit. The output is taken at Arithmetic unit with output as blocks of interpolation filters with up-sampling factors 2, 4, 8 and 16 represented by IF_2, IF_4, IF_8 and IF_{16} respectively.

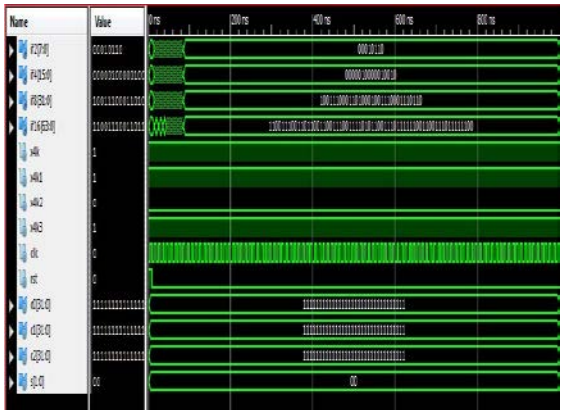

Figure 8: Final stage output for filter length, N=32

IV.CONCLUSION

An analysis of Interpolation filter with filter lengths, N=16 as well as 32 with various up-sampling factors (2, 4 and 8 for N=16; 2, 4, 8 and 16 for N=32) is performed using software tool Xilinx 14.2 ISE.

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