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Design of 64-Bit Vedic Multiplier and Square Architectures

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Abstract

The design of high speed multiplier and squaring architectures based upon ancient Indian Vedic mathematics sutras. In this work, all the partial products are adjusted using concatenation operation and are added using single carry save adder instead of two adders at different stages. The high speed Vedic multiplier architecture is then used in the squaring modules. The reduced number of computations in multiplication due to adjusting using concatenation operation and one carry save adder only. The 64 bit Vedic multiplier and squaring architectures are designed by using Xilinx Spartan-3E FPGA.

Keywords: Urdhava-Tiryakbhyam, Dwandwa-yoga, Multiplier, Square, IXI.

1. Introduction

The word '*Vedic*' was driven from the word '*Veda*' which is ancient store-house of all knowledge. Vedic mathematics provides the solution to the problem of long computation time by reducing the time delay needed for the operations to be performed. It has originated from "*Atharva Vedas*" the fourth Veda. *Atharva Veda* mainly deals with the branches like engineering, mathematics, sculpture, medicines and all other sciences. *Vedic* mathematics deals with all areas of mathematics either it is pure or applied. It was rediscovered from the Vedas between 1911 and 1918 by Sri Bharati Krishna Tirtha Ji. *Vedic* mathematics has been formulated on sixteen sutras and thirteen sub-sutras. These sutras offer magical short cut methods to all basic mathematical operations. All the advantages drives from the fact that *Vedic* mathematics approach is totally different & considered very close to the way a human mind works. *Vedic* mathematics can be applied to every branch of mathematics including arithmetic, algebra and geometry. The powerful applications of *Vedic* mathematics are in fields of Digital Signal Processing (DSP), Chip Designing, Discrete Fourier Transform (DFT), High Speed Low Power VLSI Arithmetic and Algorithms and encryption systems [1]. Arithmetic Logic unit (ALU) is the important unit in processors that performs basic arithmetic operations like addition, subtraction, multiplication and logical operations. Today's processors operate at very high clock speeds. Hence it is imperative to have faster additions, multiplications,

II.VEDIC MULTIPLIER ARCHITECTURE

This section introduces multiplication operation using *Vedic IXI Methodology* and then illustrates architecture of 2x2 multiplier modules and finally architecture of multiplier. *Urdhava-Tiryakbhayam* sutra has been used for multiplication purpose. The fig. 1 explains multiplication of two decimal numbers using IXI technique:

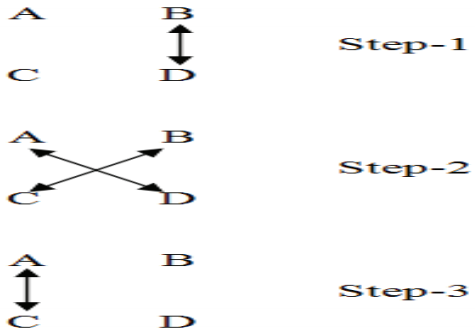

Fig. 1: IXI Methodology for Multiplication

In this method initially multiplication of the rightmost digit of multiplier is performed with the rightmost digit of the multiplicand giving the LSB of the product

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term as shown in step-1 of fig. 1. Then multiplication of the leftmost digit of the multiplicand with the rightmost digit of the multiplier and the rightmost digit of the multiplicand with the leftmost digit of multiplier is performed and then added. Thus forming the middle part of the product term as in step-2 of fig.1. At the last step, in step-3 the leftmost part of the multiplicand is multiplied with the leftmost part of the multiplier forming the leftmost part of the product term. In this way the multiplication process is carried out. Similar logic of cross multiplication and addition can be extended to implement any number of bits. Each iteration gives the coefficient of the final product.

64-bit Vedic Multiplier

This architecture consists of four 32 bit multipliers used for calculating the partial products. Next, the results of these 32 bit multipliers are adjusted using concatenation operation to have all the partial product terms of equal bit-length. The partial product of right most multiplier is concatenated with the partial product of leftmost multiplier and the partial products of middle two multipliers are concatenated with 32 zeroes each. All the numbers obtained after concatenations are added together using the single carry save adder. At the end, the sum obtained from the carry save adder is concatenated with the LSB partial product of right most multiplier to get the required final product

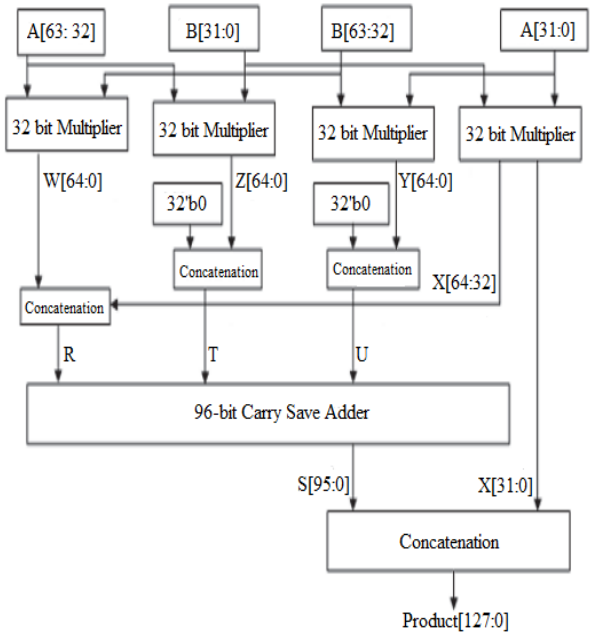


Fig 2: Architecture of 64-bit Multiplier

III. SQUARING ARCHITECTURE

Squaring is also the fundamental arithmetic operation to be performed. For squaring of a number *Urdhava-Tiryakbhyam sutra* along with *Dwandwa-yoga* is used. In this 'Duplex' technique is used. In the Duplex (D), twice the product of the outermost pair is calculated, and then added with twice the product of the next outermost pair, and so on till no pairs are left. When there is odd number of bits in the original sequence, there is one bit left in the middle, and this is entered
as its square.
For 1-bit number (X0), D = X0 * X0.
For 2-bit number (X0X1), D = 2*X1*X0.
For 3-bit number (X2X1X0), D = 2 * X2 *X0 + X1 *X1.
For 4-bit number (X3X2X1X0), D = 2 * X3 * X0 + 2 * X2 * X1.
For finding the square the duplexes are calculated starting from the either side may be left or right and is proceeded to the other direction and vice-versa. At the end duplexes are added to get the final result

64-bit Squaring Circuit

In this architecture, one multiplier of 32 bits along with two squaring circuits of 32 bits is used for the calculation of the partial products. At the last step all the calculated partial products are adjusted accordingly and are added together using the single carry save adder to get the final output.

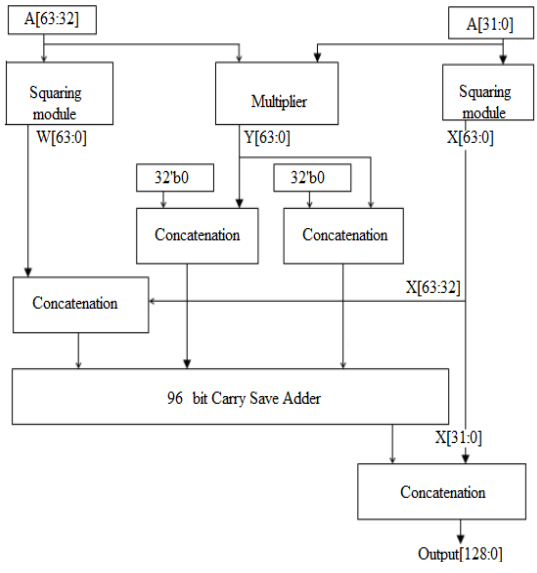
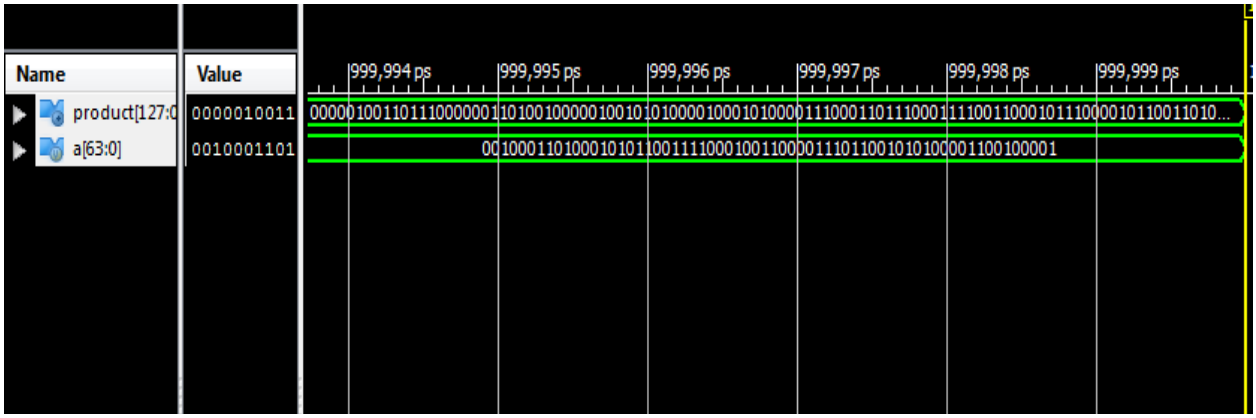


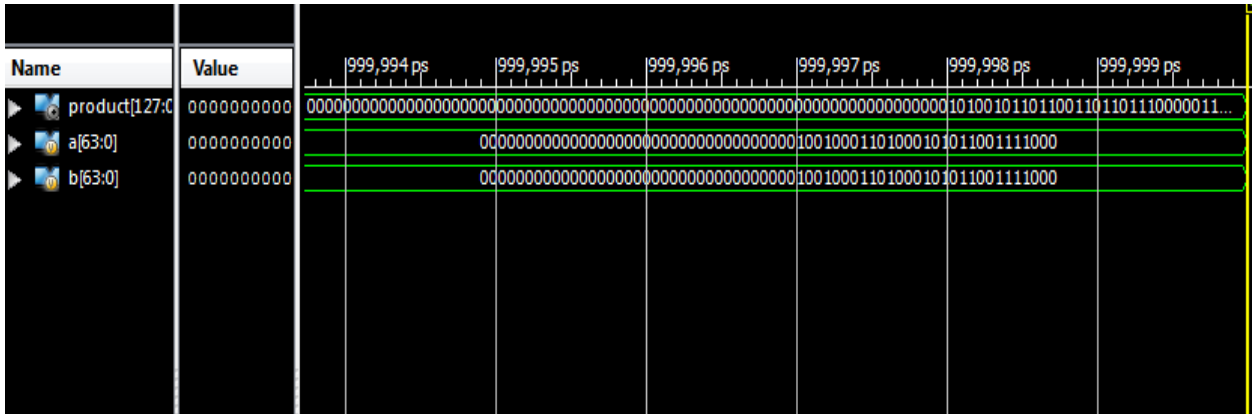
Figure 3: 64-bit Squaring Architecture

IV.SIMULATION WAVEFORMS

I. 64-bit Squaring



II. 64-bit Multiplier



V.CONCLUSION

The 64 bit Vedic multiplier and squaring architectures proved to be efficient in terms of speed. These architectures have regular structures. So, they can be realized easily on the silicon chip. The high speed Vedic multiplier architecture is then used in the squaring modules. The reduced number of computations in multiplication due to adjusting using concatenation operation and one carry save adder only. The 64 bit Vedic multiplier and squaring architectures are designed by using Xilinx Spartan-3E FPGA.

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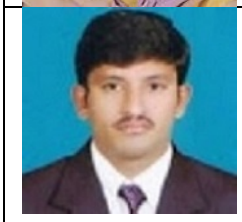	**Pathloth Krishnamurthy** is an Assistant Professor at Brilliant Institute of Engineering and Technology, Hyderabad in ECE Department. He received his B.Tech degree in Electronics and Communication Engineering from Madhira Institute of Science & Technology, Hyderabad and M.Tech degree in VLSI System Design from Joginpally Bhasker Rao Institute of Engineering & Technology, Hyderabad. His research interest is VLSI Technology and Design and Communication Systems.