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FPGA Implementation of Vedic ALU with Application Specific Reversible Gates

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Abstract

The Urdhva Triyambakam method derived from the ancient Indian mathematics will be used in the proposed project. Reversible circuits, on the other hand, reduces the power dissipation incurred due information/bits loss as in the case of an irreversible circuit making way for better power utilization . The proposed ALU design has a four bit control signal. It performs six arithmetic operations and ten logical operations. The proposed ALU uses both reversible and semi reversible gates in it. Arithmetic operations are addition, subtraction, multiplication, division, increment and decrement. Logical operations are and gate, or gate, not gate, nand gate, nor gate, xor gate, xnor gate, a'b, barrel left shifter, barrel right shifter. The operations performed based on the control bits are as follows. Total of sixteen operations are performed by the proposed ALU. The proposed ALU is coded in Verilog followed by synthesization using XilinxISE13.2i.

1. Introduction

The Primary objective of a digital circuit design is to optimize for speed, area, power and energy. While it's a challenge for circuit designers, to achieve this optimization without compensating for one or the other parameters mentioned above. Certain design techniques, algorithms and smarter planning of the available resources have proven to be successful to achieve the level of optimization required for much higher efficiency. Arithmetic Logic Unit (ALU) being the driving component of a processor, optimizing its module for speed and power becomes quite inevitable. Many previously published technical papers have emphasized the use of reversibility in circuits design for reduction in power dissipation, while successfully demonstrating the same. However this reduction in power was also followed by significant reduction in speed as well as increase in chip area. Hence smarter algorithm and logic design was required to speed up the execution of a logic module. With this reference, 'Vedic Algorithm' technique was utilized to pave way for faster execution of an arithmetic module of an ALU. While there are as many as 16 techniques(sutras) in the Vedic algorithm, the proposed design will implement multiplier using the popular Urdhva method (Urdhva Triyambakam) along with certain improvisation while designing the same, further details of which is explained in the subsequent parts of the paper. The conventional way of implementing the multiplier would have involved series of AND gates and adders to get the required output while incurring significant delay. The Vedic algorithm provides a faster way to get through the output with less number of logical elements involved, thereby reducing the delay while effectively increasing the speed of processing the output. A simple illustration of Vedic technique is explained in the figure.

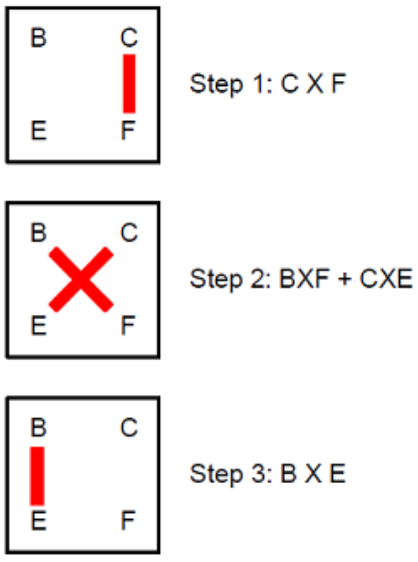

Figure 1: Multiplication Technique Using Urdhva Triyambakam Sutra

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II. **Reversibility**

The strengths of Reversibility in digital circuits is well documented and explained by R. Launder [9] in his article. A circuit which can undo or reverse its output to get back its original input will not suffer infonnation loss, since all the information are present within the circuit and only need to be reversed, to be recovered. Hence a reversible circuit will save major chunk of power dissipation suffered due to information loss that happens every clock cycle.

The basic requirement of a reversible circuit is to have a one-to-one correspondence between inputs and outputs, which requires the input and output pin count to be same. Also each input state must correspond to a particular unique state of the output i.e. output states cannot be shared by more than one input states available. If the above criteria are satisfied the inverse circuit can be easily designed to make the circuit reversible.

I. Reversible Gates

The reversible gates used in this paper are as follows.

Peres Gate

Peres gate is a 3x3 reversible gate. The quantum cost of this gate is 4. It is mainly used for half adder application. It has lesser area and quantum cost compared to other reversible gates like Fredkin and Feynman gate. It has three inputs A, B and C. The outputs are given as P=A, Q=A xor B and R= (A.B) xor C. To use it as an half adder C is given logical zero. The outputs of the gate become P=A, Q=A xor B and R=A.B.

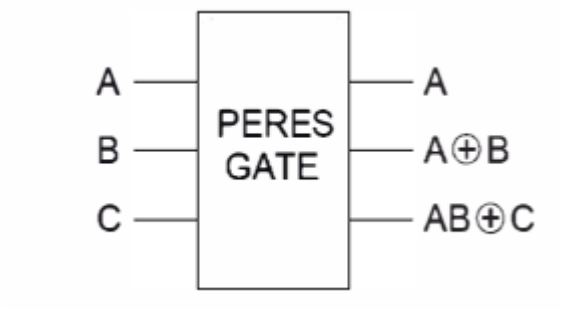


Fig 2: Peres Gate

HNG Gate

HNG gate is a 4x4 reversible gate. It is mainly used for full adder application. The quantum cost of this gate is 6. It has four inputs A, B, C and D. The outputs are given as P=A, Q=B, R=A xor B xor C and S= (A xor B).C xor (AB xor D). To use it as a full adder D is assigned to logical zero and C is assigned the input carry bit. The outputs of the gate become P=A, Q=B, R= A B C and S= (A xor B).C xor AB.

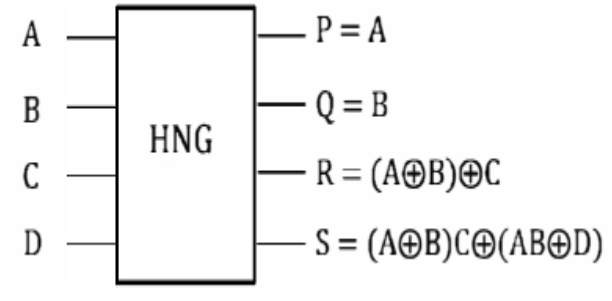


Fig 3: HNG Gate

BJN Gate

It is a 3x3 reversible gate. The quantum cost of this gate is 5. For the three inputs A, B and C the outputs are P=A, Q=A and R= (A+B) xor C. In this paper it is used in the logical unit. This gate is used to realize OR and NOR gates. When C=O, R= (A+B) and for C=l, R= (A+B).

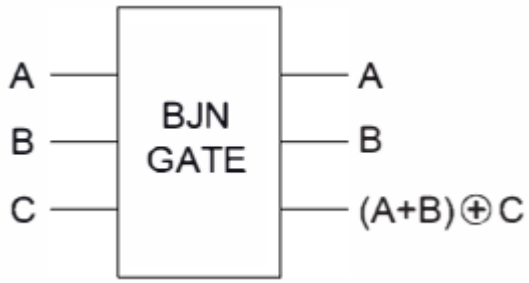


Fig 4: BJN Gate

TSG Gate

It is a 4x4 reversible gate. This gate can realize most of the Boolean logical operations like AND, NAND, XOR, XNOR and NOT. The outputs of this gate are P=A, Q=A'C' xor B', R= (A'C' xor B') xor D and S= (A'C' xor B') D xor (AB xor C). Inputs C and D are used as control signals to select the logical operation.

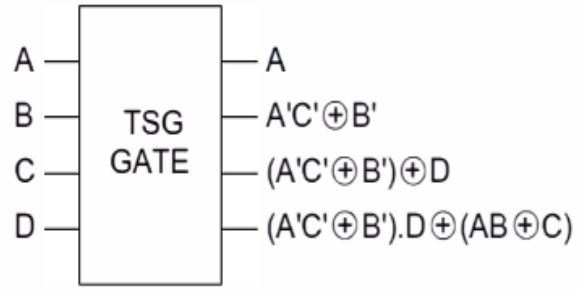


Fig 5: TSG Gate

II. Arithmetic unit

Full Adder/Subtractor

This adder is a 4-bit ripple carry adder. It is made using four HNG gates. HNG gates have the minimum delay, area and quantum cost for full adder application. The two inputs and carry bit is given to the first, second and third input respectively of the HNG gate. The fourth input pin of this HNG gate is grounded so it acts as a full adder. The output bits of the HNG will be P=A, Q=B, R= (A xor B) xor C, S= (A xor B).C xor AB. R is the sum of the addition and S is the carry. A control signal S is used to switch between adder and subtractor mode. When S=0, the circuit acts as a 4-bit full adder. When S=1, input b is complemented and an input high carry bit is given to the LSB full adder. In subtractor, R is the difference and S is the borrow bit. If the result of the 4-bit subtraction is negative then the borrow will be zero and output is stored as 2's complement.

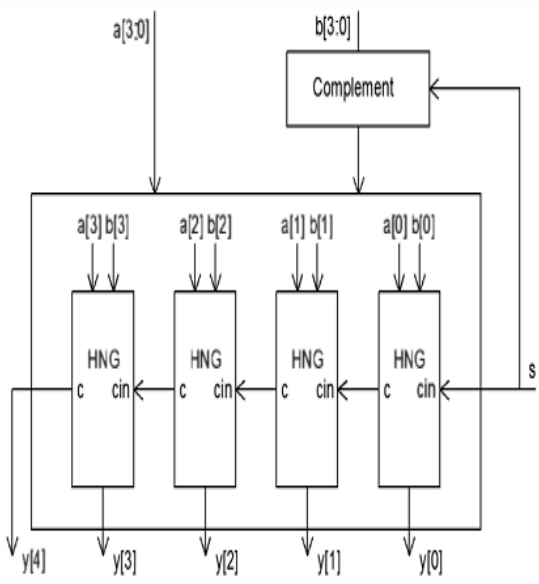


Fig 6: Reversible Full Adder/Subtractor

Proposed KSA Gate

It is a 4x7 semi-reversible logic gate designed especially for 2-bit multiplication application. Out of the seven outputs, the first four outputs give the product of the two 2-bit inputs assigned to the four input pins. Three more output pins are added to make one-to-one mapping between inputs and outputs. Since this gate has 7 output bits it is expected to have one-to one mapping between all the 128 cases. The proposed semi-reversible gate has one-to-one mapping between the inputs and outputs for the possible 16 cases of output product. Using a general purpose reversible gate for a specific application has more number of redundant gates and garbage outputs.

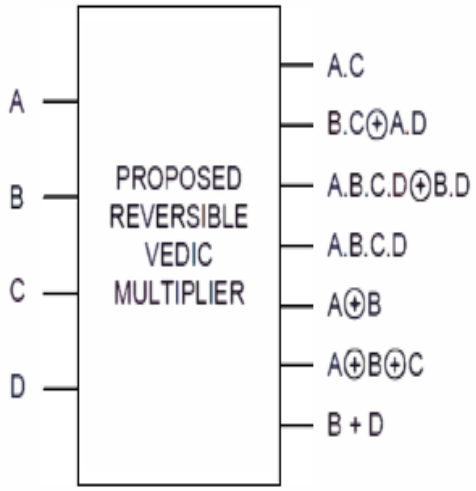
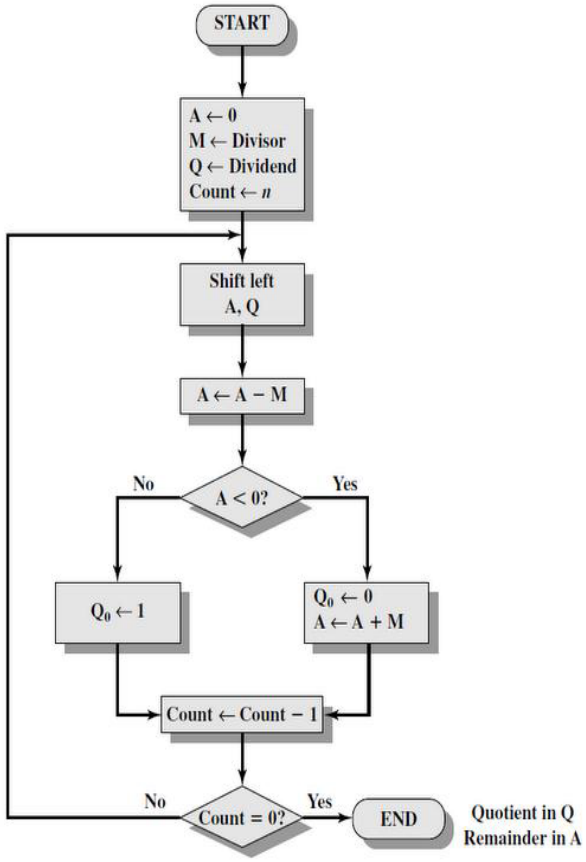


Fig 7: TSG Gate Proposed KSA Gate

Division



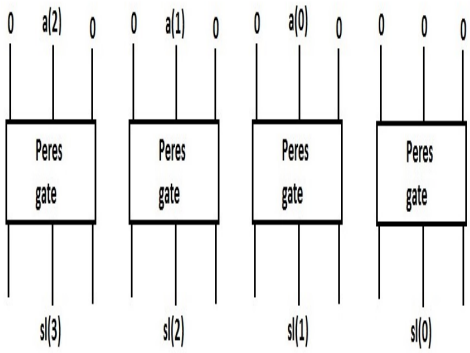
In this division block, HNG gate is used as adder/subtractor. In this Shift block, PERES gate is used.

III.Logical Unit

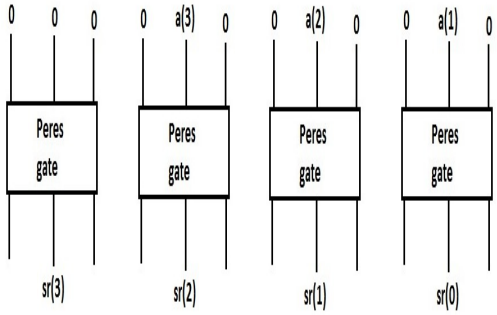
The proposed 4-bit logic unit performs the logic operations on two 4-bit numbers. The 8 basic logic operations performed by proposed logic unit are AND, NOR, XNOR, XOR, NOT (invert), NAND, A'B, OR, NOR etc. A BJN gate is used to implement OR and NOR operations.

A control input C controls the operation of a BJN gate. When C=O, BJN gate performs OR operation of two inputs A and B. When C=l, it gives NOR operation of A and B. TSG gate is used to implement the rest of the logical operations. Input C and D acts as control signals to TSG gate. When c=o and D=O, it results in AND operation of A and B. When c=o and D=l, it gives XOR and XNOR operations of A and B. When C=1and d=0, the resulting output is inversion of B and NAND operation of A and B. When C=1and d=1, it results in A'B. Thus overall logic unit uses only two types of reversible gates to implement 8 logic operations

Barrel left shifter



Barrel right shifter



IV.ALU DESIGN

The proposed ALU design has a four bit control signal.

- It performs six arithmetic operations and ten logical operations.
- The proposed ALU uses both reversible and semi reversible gates in it.

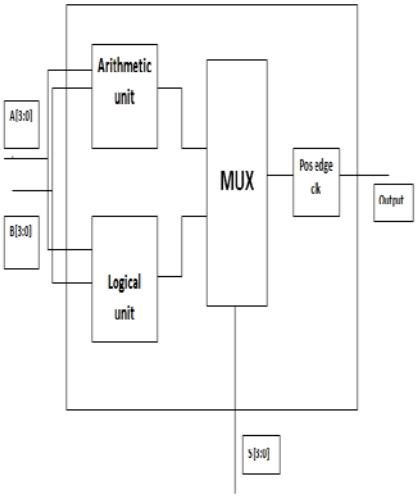


Fig 8: Proposed Architecture of ALU

The operations performed based on the control bits are as follows. Total of sixteen operations are performed by the proposed ALU.

Table 1. Operations performed based on the control signal

Control Signal	Operation
0000	Addition
0001	Subtraction
0010	Multiplication
0011	Division
0100	Increment
0101	Decrement
0110	And
0111	Xor
1000	Xnor
1001	Not
1010	Nand
1011	A'B
1100	Or
1101	Nor
1110	Barrel Left Shifter
1111	Barrel Right Shifter

V. Simulation Results

Fig 9: Reversible ALU

Fig 10: Division Operation

Fig 11: Shift Operations

VI. Synthesis Results

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Device utilization summary:
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Selected Device : 3s500efg320-4

 Number of Slices:                       50  out of   4656     1%
 Number of 4 input LUTs:                 91  out of   9312     0%
 Number of IOs:                          21
 Number of bonded IOBs:                  20  out of    232     8%

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Partition Resource Summary:
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  No Partitions were found in this design.

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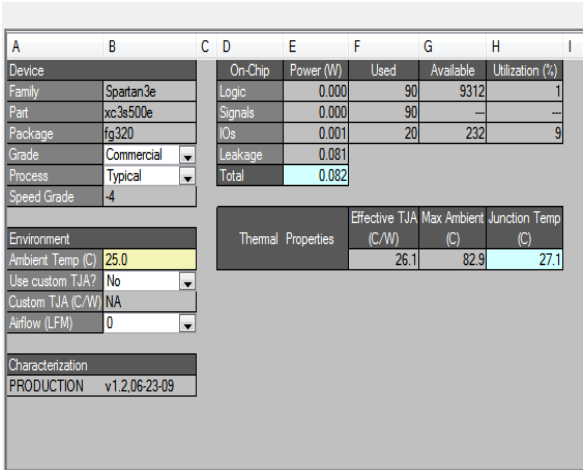
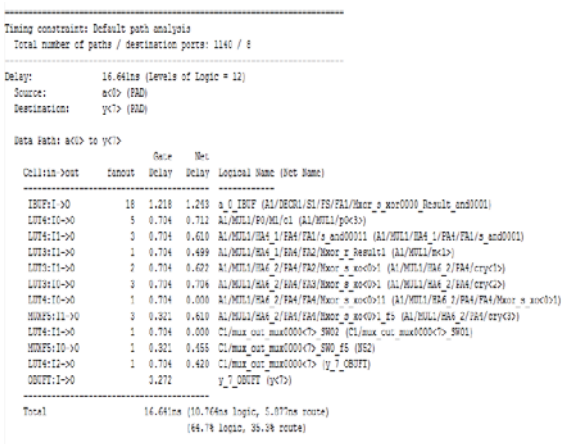
Fig 12: Area of Reversible ALU



A	B	C	D	E	F	G	H	I
Device			On-Chip	Power (W)	Used	Available	Utilization (%)	
Family	Spartan3e		Logic	0.000	90	9312	1	
Part	xc3s500e		Signals	0.000	90	--	--	
Package	fg320		IOs	0.001	20	232	9	
Grade	Commercial		Leakage	0.081				
Process	Typical		Total	0.082				
Speed Grade	-4							
			Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)		
Environment				26.1	82.9	27.1		
Ambient Temp (C)	25.0							
Use custom TJA?	No							
Custom TJA (C/W)	NA							
Airflow (LFM)	0							
Characterization								
PRODUCTION	v1.2,06-23-09							

Fig 13: Power of Reversible ALU



```
Timing constraint: Default path analysis
  Total number of paths / destination ports: 1140 / 8
-------------------------------------------------------------------------
Delay:               16.641ns (Levels of Logic = 12)
  Source:            a<0> (PAD)
  Destination:       y<7> (PAD)

  Data Path: a<0> to y<7>
                                        Gate    Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             18   1.218   1.249  a_0_IBUF (A1/DECRL1/S1/FS/FA1/Mxor_s_xor0000_Result_and0001)
     LUT4:I0->O             5   0.704   0.712  A1/MUL1/P0/M1/o1 (A1/MUL1/p0<3>)
     LUT4:I1->O             3   0.704   0.610  A1/MUL1/HA4_1/HA4/FA1/s_and00011 (A1/MUL1/HA4_1/HA4/FA1/s_and0001)
     LUT3:I1->O             1   0.704   0.499  A1/MUL1/HA4_1/HA4/FA2/Mxor_r_Result1 (A1/MUL1/Mx1>)
     LUT5:I1->O             2   0.704   0.622  A1/MUL1/HA4_2/HA4/FA2/Mxor_s_xo<0>1 (A1/MUL1/HA4_2/FA4/cryc<5>)
     LUT3:I0->O             3   0.704   0.706  A1/MUL1/HA4_2/HA4/HA3/Mxor_s_xo<0>1 (A1/MUL1/HA4_2/HA4/cryC2>)
     LUT4:I0->O             1   0.704   0.000  A1/MUL1/HA4_2/HA4/FA4/Mxor_s_xo<0>11 (A1/MUL1/HA4_2/FA4/FA4/Mxor_s_xo<0>1)
     MUXF5:I1->O            3   0.321   0.610  A1/MUL1/HA4_2/HA4/HA4/Mxor_s_xo<0>1_f5 (A1/MUL1/HA4_2/HA4/cryC3>)
     LUT4:I1->O             1   0.704   0.000  C1/mux_out_mux0000<7>_SW02 (C1/mux_out_mux0000<7>_SW01)
     MUXF5:I0->O            1   0.321   0.455  C1/mux_out_mux0000<7>_SW0_f5 (N52)
     LUT4:I2->O             1   0.704   0.420  C1/mux_out_mux0000<7> (y_7_OBUFT)
     OBUFT:I->O                 0.272          y_7_OBUFT (y<7>)
    ----------------------------------------
    Total                      16.641ns (10.764ns logic, 5.877ns route)
                                       (64.7% logic, 35.3% route)
```

Fig 14: Delay of Reversible ALU

VII.COMPARISION

Parameter	Normal 4-bit ALU	Reversible 4-bit ALU
LUTs used(area)	102	91
Power dissipation(W)	0.088	0.082
Delay(ns)	15.264	16.642

VIII.CONCLUSION

The proposed ALU design has a four bit control signal. It performs six arithmetic operations and ten logical operations. The proposed ALU uses both reversible and semi reversible gates in it. Arithmetic operations are addition, subtraction, multiplication, division, increment and decrement. Logical operations are and gate, or gate, not gate, nand gate, nor gate, xor gate, xnor gate, a'b, barrel left shifter,

barrel right shifter. The operations are performed based on four control bits using mux. Total of sixteen operations are performed by the proposed ALU. The Reversible ALU occupies less area and consumes less power compared to normal ALU. The proposed ALU is coded in Verilog followed by synthesization using XilinxISE13.2i.

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