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# RF Front-end Design of a Digital TV Receiver

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**Abstract**

This paper presents a RF Front-end of Digital TV Receiver the frequency swept from 100MHz to 1.2GHz in CMOS process. This Front-end is designed by using Inverter with Self bias Current reuse LNA and Mixer which consumes power of 14.79 mw from 1.8V supply. The Front-end has good linearity 1dB compression point is -33.7 dBm, Input-referred third-order intercept point (IIP3) is -11.54 dBm.It has low Noise figure of 4 dB ,S11 is -16 dB and high gain .So it is suitable for Digital TV applications

**Keywords:** self bias, current reuse,1 dB compression point and input-referred third-order intercept point

## Introduction

DTV signals have advantages of high quality and bandwidth efficiency, so analog TV broadcasting services are replaced by digital TV broadcasting services. Accordingly, DTV tuners are widely used in the TV tuner market. Most terrestrial and cable DTV standards such as Digital Video Broadcasting (DVB) and Advanced Television Systems Committee (ATSC) use broadband frequencies from 54MHz to 882MHz. Many existing wireless systems are overlap in the frequency range 0–960 MHz, e.g., VHF and UHF TV channels from 54 to 890 MHz and cell phone bands around 850 MHz and 900 MHz. when most of the interferers are in-band, the concern of folding out-of-band interference in band and swamping the signal due to nonlinear intermodulation also diminishes [3].So RF front end design of DTV receiver frequencies from 100MHZ to 1.2GHZ to overcome these problems.

When the signal is transmitted through wireless media it has to be travel some distance so the transmitted signal has high frequency. RF-front end design has LNA and Mixer, this is used in Digital TV Receivers.LNA is main building block in design of receivers. Generally in design of Digital TV Receivers will get some external noise and system noise.LNA is used to reduce the system noise. The incoming signal is first amplified with an LNA. The output of the amplifier is down converted in mixer which uses local oscillator, synchronized in freq to the carrier of desired signal, then will get baseband signal. In the design of LNA inductor is used but it takes more area to eliminate this inductor less LNA is used. but rather to minimize the power consumption while achieving a moderate noise figure and linearity [4]. There are many topologies which can realize single-ended LNA, the resistive feedback topology LNA has good input match but low NF[2].The Inductive source degeneration topology LNA has good narrow band matching ,low NF but large area. The common gate topology LNA has good input matching but huge NF and low power. However, in order to obtain low noise, high gain and good input matching [5].The LNA designed by inverter with resistive feedback has low gain.[1]. The wideband LNA is flexible and efficient in terms of area and power. One technique is that to lower the power consumption reuse the current by stacking the nMOS and pMOS transistors used as amplifying devices [12].

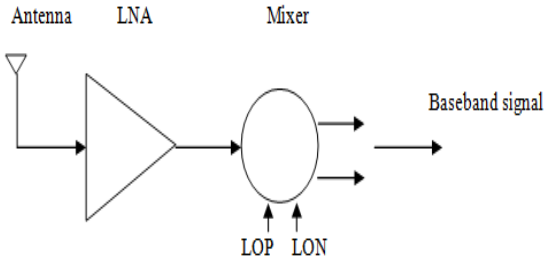


**Figure 1: Block Diagram of RF Front-end design of Digital TV Receiver**



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A PMOS transistor is stacked on top of the nMOS transistor, which helps to enhance the overall transconductance from gm to gmn+gmp approx (2gm) and allows one to halve the current from resistance [11].

In this paper, we present a two stage LNA. The first stage is that inverter with self bias to achieve high gain and input matching; the second stage is to work LNA in both low gain and high gain mode. It uses current reuse technique. Mixers are crucial parts of any typical front end circuit. Mixer follows LNA this should have excellent linearity and low noise figure. The front-end design shown in Fig.1.The gain of the mixer has to be increased to suppress the high noise level [4].Conversion process is performed by multiplying the RF signal by a signal named Local (LO). Nonlinearity effect of the mixer is necessarily considered for this frequency translation to produce sum and difference of frequencies. But it also has disadvantages like High LO to IF feed-through, large power consumption compared to previous topology and noise figure increases. To overcome these problems single balanced mixer is designed. It has Tran's conductance amplifier which convert voltage to current and two switching stages are involved.

## II CIRCUIT DESIGN AND ANALYSIS

In this paper **Front**-end of Digital TV receiver designed by Low noise amplifier and Mixer at supply voltage 1.8 V, the frequency swept from 100MHz to 1.2GHz. Low noise amplifier is designed in two stages inverter as input stage and current reuse technique used with self bias resistor. Mixer is designed by using Tran's conductance amplifier and RC loading stages.

### A. Inverter with self bias current reuse LNA

The CMOS LNA for 100 MHz-1.2 GHz is operated in 1.8 V is shown in Fig.2 for low gain and high gain mode. It consists of two stages. The first stage uses inverter with self bias R1 is to amplify the received signal with input impedance matching and low noise figure. The low power technique in LNA design is by means of inverter with self bias by current reuse technique. In the first stage C1 should be high, resistance R1 must be select as to get the required frequency minimum 100MHZ. The inverter stage is easy to operate because it is just depend upon the bias conditions. If M1 and M2 are in saturation region then will chance to get maximum gain.

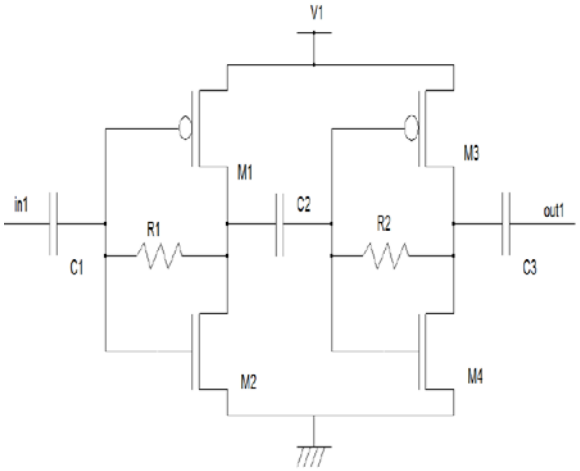


**Figure 2: Schematic of current reuse LNA**

The input impedance matching is done by using transconductance (2/(gmn+gmp),2/2gm) 1/gm .The input matching for LNA is shown in Fig.3.The capacitance C2 is used to bias the signal it allows AC signal and blocks DC signal. The second stage employs the inverter to work the LNA in both low gain and high gain mode. The gain for LNA is

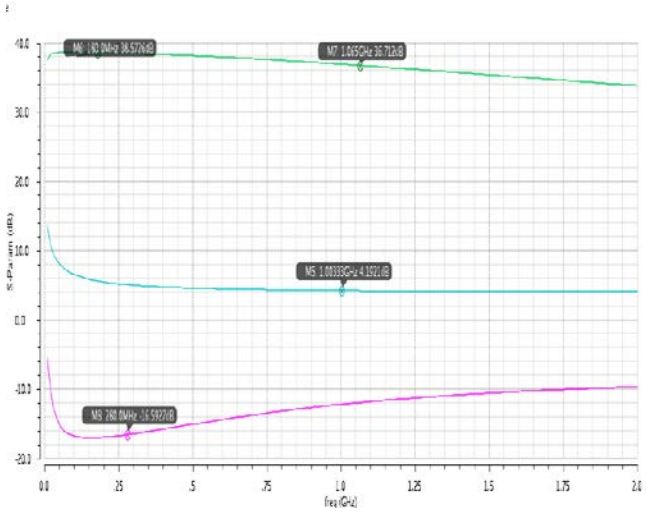

**Figure 3: Gain, Noise figure, S11 of current reuse LNA**

shown in Fig.3.The M3 and M4 are reuse the current by first stage.The resistance R2 is varying to work the LNA in both low gain and high gain mode. If the capacitance C3 is the next block, the output matching is not necessary in the design of LNA. The Noise figure for LNA is shown in Fig.3.So that the LNA achieves low noise figure,good input matching and high gain.

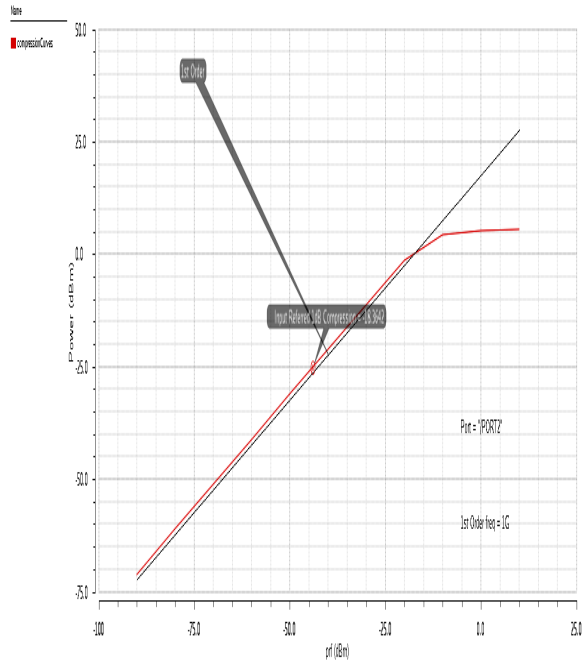


**Figure 4: 1dB compression point of current reuse LNA**

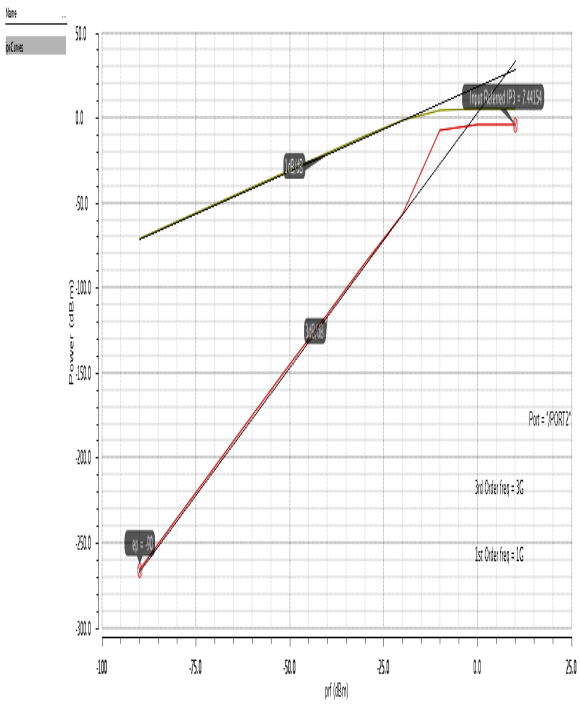


**Figure 5: Input-referred third-order intercept point (IIP3) of current reuse LNA**

**B. Mixer**

The RF input in1 is biased with voltage biased circuit and to match the RF input stage, RC Matching is used. The two switches M6 and M7 are driven by differential LO phases LOP and LON, thus "commutating" the RF input to the two outputs, called a single-balanced mixer because of the balanced LO waveforms, this configuration provides twice the conversion gain of the mixer. The circuit naturally provides differential outputs even with a single-ended RF input in1.The RF output out1 is given as input to the mixer .The transconductance amplifier convert the voltage to the current. The current is used in the next stages. The switches M6 and M7 are given to LOP and LON to remove the noise in clock signal .RC loading stages are used to increase the overall gain in the output .Schematic of Mixer shown in Fig.6. A good mixer is highly linear, and its input-referred noise does not overwhelm the amplified noise of the preceding LNA.

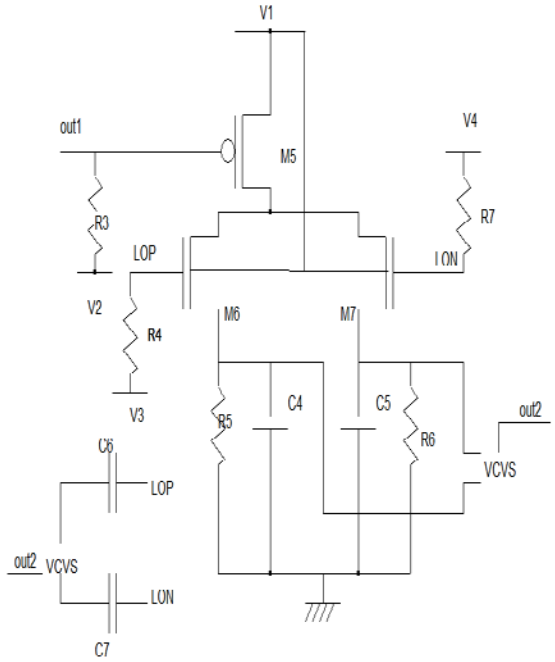


**Figure 6: Schematic of Mixer**

**III EXPERIMENTAL RESULTS**

The proposed DTV receiver front-end was implemented using CMOS process. The Low Noise Amplifier and single balanced mixer consume 8 mA, 0.22mA respectively. The total current consumption is approximately 8.22 mA, at a supply voltage of 1.8 V. The input matching is less than 16 dB over all TV Bands. The input frequency was from 100 MHz to 1.2GHz. The LNA NF is 4 dB over the TV bands.The LNA 1 dB compression point is -18.36 dBm and input referred third order intercept point is (IIP3) is 7.44 dBm are shown in Fig.4 and Fig.5 . The 1 db compression point is -36.7 dBm and IIP3 -11.54 dBm

are obtained for front-end of Digiatl TV Receiver are shown in Fig.7 and Fig.8. This linearity performance meets the selectivity test patterns for DTV receivers. Conversion gain of RF front-end is 43.52 dB is shown in Fig.9.. Table I shows the comparison of parameters like supply voltage, technology, frequency, voltage gain, power consumption, noise figure,IIP3 etc. of various Front-end design of receivers.

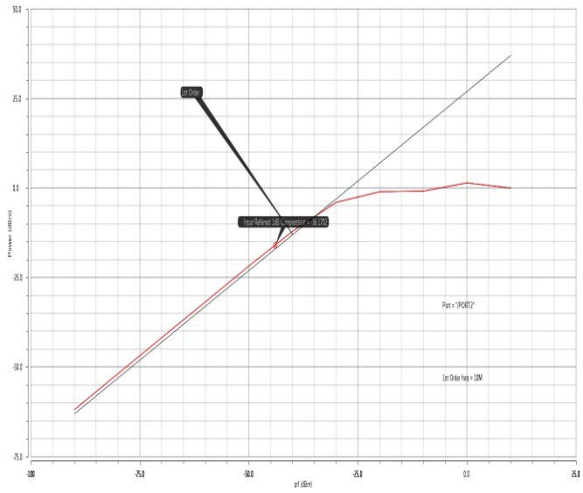

**Fig.7 1dB compression point for Front-end of Digital TV Receiver**

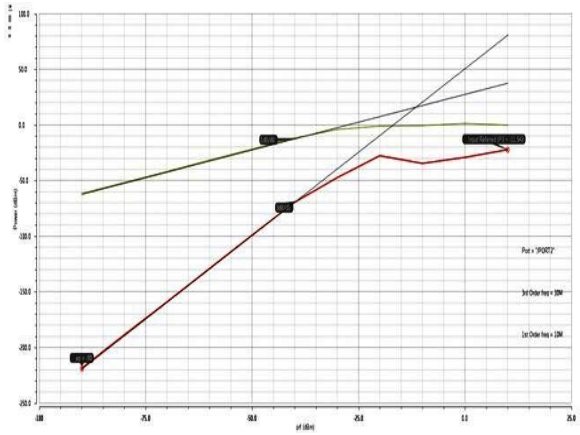

**Fig.8 Input-referred third-order intercept point (IIP3) for Front-end of Digital TV Receiver**

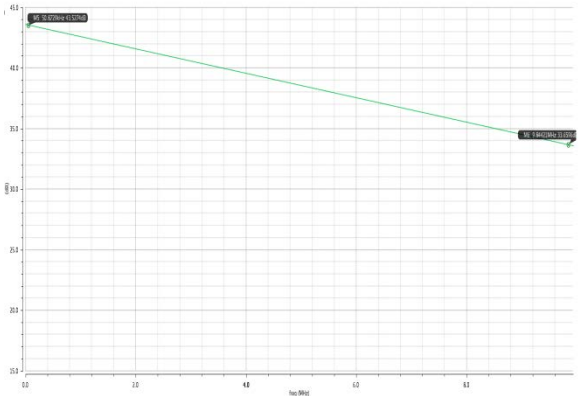

**Fig.9 Conversion gain for Front-end of Digital TV Receiver**

**TABLE 1: Comparison of Various parameters in Front-end of Receiver**

| S. No. | Technique | Technology | Voltage supply(v) | Frequency (GHz) | Voltage gain(dB) | Power consumption(mW) | Noise figure (dB) | IIP3 (dBm) |
|---|---|---|---|---|---|---|---|---|
| 1 | Single-to-Differential LNA for Digital TV Receiver[1] | 0.18 µm CMOS process | 1.8 | 1 | 16.4 | 12.8 | 3 | -13.3 |
| 2 | Direct conversion wireless Receiver[14] | 1µm CMOS process | 3 | 1 | 20 | 27 | 3.2 | +8 |
| 3 | Low –IF receiver[15] | 0. µm CMOS process | 3.3 | 2.4 | 60 | 115.5 | 7.2 | -3.4 |
| 4 | Double balanced CMOS Receiver[16] | 180nm CMOS process | 3 | 1.8 | 15 | 75 | 2.1 | +10 |
| **5** | **LNA in Digital TV Receiver(This paper)** | **180nm CMOS process** | **1.8** | **1.2** | **36** | **14.4** | **4** | **+7.4** |
| **6** | **Front-end of Digital TV Receiver(This paper)** | **180nm CMOS process** | **1.8** | **1.2** | **43.5** | **14.79** | **6** | **-11.5** |

## IV. CONCLUSION & FUTURE SCOPE

This paper RF front-end for the DTV receiver presents the low power consumption ,high gain using a CMOS process. The proposed RF front-end consists of a current reuse two stage LNA, a single balanced mixer. The Low noise amplifier gain increases by 20 dB compared to single to differential LNA. Because of current reuse technique Trans conductance increases, gain increases. The Conversion gain 43.52 dB is achieved. The power consumption is increased by 1.6 mW compared to single to differential LNA, because of high gain. It obtains excellent selectivity (high linearity). Total current consumption is 8.22 mA at supply voltage of 1.8 V is obtained. This project can be extended by design of Digital TV tuner by using the inductor less single ended LNA and Mixer ,the frequency swept from 100MHz to 1.2GHz.

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