ISSN: 2456-043X

International Journal of Engineering Science and Generic Research (IJESAR)
Available Online at www.ijesar.in
Volume 2; Issue 4; July-August; 2016; Page No. 55-61

FPGA based Performance Analysis of Micro programmed FIR Filters using Multipliers

Pathapati Tanuja[1], B.Bhavani [2]

[1]Department of ECE, MVSR Engineering College, Hyderabad, India

(PG Scholar)

[2]Department of ECE, MVSR Engineering College, Hyderabad, India

(Assistant Professor)

pathapati.tanuja@gmail.com

Abstract

The micro architecture of digital FIR filter consists of a data path and a control unit. The data path is the computational engine of FIR filter and mainly consists of adders, multipliers and delay elements. The hardware implementation of a Sequential and parallel digital FIR filter architecture using a novel micro programmed controller is presented. The main advantage of the micro programmed controller is its flexibility in modifying the micro program stored in ROM based control memory. To improve the performance of FIR filter, an efficient multiplier is required. Wallace tree and Vedic multipliers are used for the implementation of sequential and parallel micro programmed FIR filter architectures we have proposed a novel high speed and area efficient Vedic multiplier using compressors is used for the implementation of sequential and parallel micro programmed FIR filter architectures. The proposed technique, a 4-tap sequential and parallel FIR filter is implemented using Xilinx Spartan 3e FPGA. The proposed FIR filter is coded in VERILOG. The design can be easily modified to implement higher-order and high speed FIR filters which are commonly used in video and image processing applications.

I. Introduction

Digital filters are normally used to filter out undesirable parts of the signal or to provide spectral shaping such as equalization in communication channels, signal detection or analysis in radar applications. Adders, multipliers and shift registers are the basic building blocks commonly used in the implementation of digital filters. Different architectures of digital filters can be realized to achieve the same transfer function. The architectures possess different attributes in the form of speed, complexity and power dissipation [1].Finite impulse response (FIR) and infinite impulse response (IIR) are two such filters used in different applications.

FIR filters are the important building blocks for digital signal, video and image processing applications. Basically, FIR filter performs a convolution on a window of *N* data samples. A common implementation of the FIR filter is shown in fig. 1, which is also known as direct form FIR filter. As can be seen from the figure, *N*-tap or (*N*-1)th order FIR filter consist of *N* shift registers, *N* multipliers and *N*-1 adders. The impulse response of the FIR filter can be directly inferred from the tap coefficients (*W*).

The multiplier is the fundamental component which decides the overall performance of the FIR filter [2].

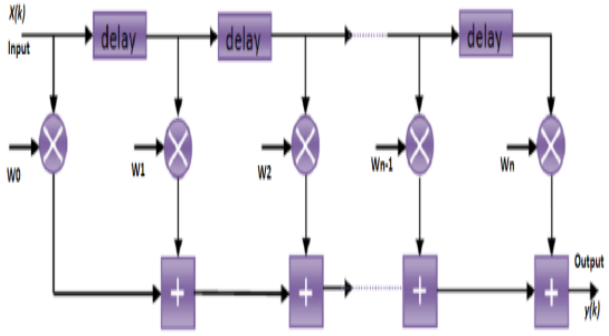


Fig 1: Direct form FIR filter

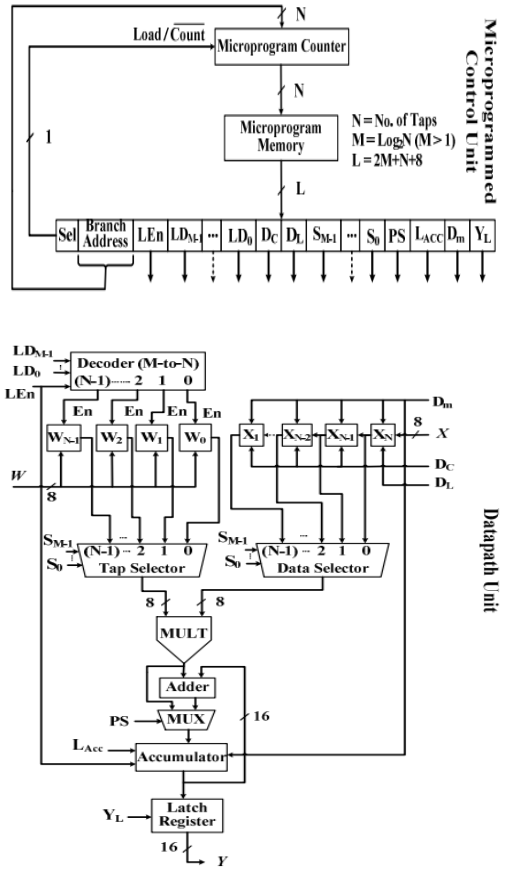
II. MICRO PROGRAMMED FIR FILTER

The micro programmed FIR filter consists of a data path and a micro program control unit (MCU). The most important advantage of the MCU is its flexibility.

Corresponding author: Pathapati Tanuja

I. Sequential Architecture of Micro programmed FIR Filter

The sequential architecture of *N*-tap micro programmed FIR filter is shown in Fig. 2. It basically comprises of a MCU and a data path unit. The MCU consists of a microprogram counter and microprogram memory. The data path unit comprises of 2*N* data (X) and coefficient (W) registers and *M*-to-*N* decoder (*M* = *log2N*), two *N*-input multiplexers for selecting the data and coefficients, a multiplier and an adder, a two input multiplexer to control the flow of data from multiplier or accumulator, one 16-bit accumulator and a 16-bit register to latch the data [8].



Controls signals for data path unit

Fig 2: Architecture of sequential micro programmed FIR filter

II. Parallel Architecture of Micro programmed FIR Filter

The parallel architecture utilizes multiple adders and multipliers, based on the size of the FIR filter, in contrast to single adder and multiplier used in the sequential architecture design. Fig. 3 illustrates the parallel architecture of then micro programmed FIR filter [8]. The data path micro architecture of 4-tap parallel FIR filter consists of the following sub-modules: Four 8-bit data registers, One 2-to-4 decoder, Four 8-bit coefficient registers, Four multipliers (8×8),Three 16-bit adders, One 16-bit register for latching the output.

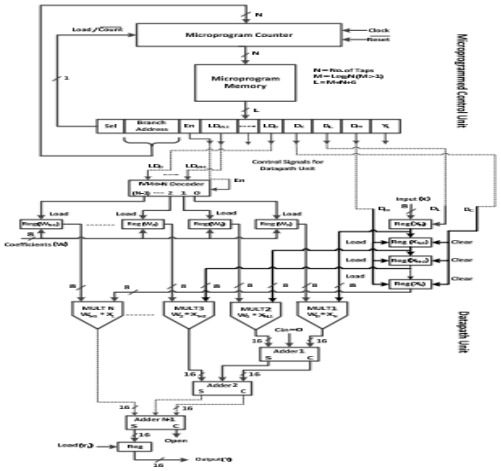


Fig 3: Architecture of parallel micro programmed FIR filter

III. WALLACE TREE MULTIPLIER DESIGN

A method for fast multiplication was originally proposed by Wallace [9]. Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. Using this method, a three step process is employed to multiply two integer numbers. The first step is to multiply each bit of one of the arguments, by each bit of the other, yielding *n2* results.

The second step is to reduce the number of partial products to two by layers of full and half adders. The third step is to group the wires in two and then add them using conventional adder [10]. In this paper, two different architectures of Wallace tree multiplier are presented.

First one is designed using only half adder and full adder, while the second one uses a more sophisticated carry skip adder (CSA) [11].

I. Wallace Tree Multiplier using Full and Half Adders

The Wallace tree method reduces the number of adders by minimizing the number of half adders in any multiplier. In 8×8 multiplier, the first partial

product is the least significant bit in the output of the multiplier result. After that, moving to the next column of the partial product if there are any adders from the previous product, the full adder is used otherwise a half adder is used and so on.
Fig. 4 shows how the algorithm is implemented [10].

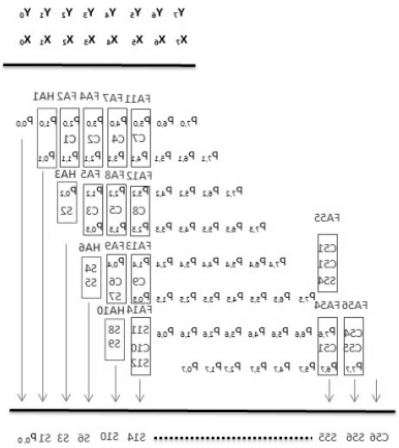


Fig 4: Wallace Tree partial Using half and full adders.

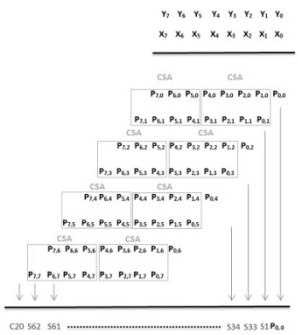


Fig. 5. Wallace Tree using Carry skip adder.

II. Wallace Tree Multiplier using Carry skip adder

In this design, 4-bit carry skip is used for the addition of partial products. Four bits from one row is being added with the next row as shown in Fig. 5 and the carry output from the first addition is the carry input for the second addition. The main advantage of using CSA is to improve the speed.

IV. VEDIC MULTIPLIER DESIGN

Vedic mathematics is an ancient form of mathematics which was developed in India by *Sri Bharati Krishna Tirthaji*, a renowned Sanskrit scholar and mathematician of his times. It is based on sixteen Sutras or algorithms [12]. *Urdhva Tiryakbhyam Sutra* (vertically and crosswise algorithm) is used for efficient digital multiplication. Its calculation is defined by vertical and crosswise product that gives advantage over the normal conventional horizontal multiplication. For binary number, the multiplication operation is reduced to bitwise “AND” operation and the addition operation use full or half adders.

As mentioned earlier, Vedic Mathematics can be divided into 16 different sutras to perform mathematical calculations. Among these the Urdhwa Tiryakbhyam Sutra is one of the most highly preferred algorithms for performing multiplication. The algorithm is competent enough to be employed for the multiplication of integers as well as binary numbers. The term "Urdhwa Tiryakbhyam” originated from 2 Sanskrit words Urdhwa and Tiryakbhyam which mean “vertically” and “crosswise” respectively [7]. The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques, is the fact that it utilizes only logical “AND” operations, half adders and full adders to complete the multiplication operation. Also, the partial products required for multiplication are generated in parallel and apriori to the actual addition thus saving a lot of processing time.

The Vedic mathematics concept is applied to develop modular RTL Verilog code for 2×2 multiplier which can be used as a building block to develop 4×4 multiplier. An 8×8 multiplier can be further designed using the 4×4 multiplier and so on.

The 4-bit and 8-bit multipliers used Ripple carry adder for the proposed design. The same Vedic multiplier design is realized using Kogge-Stone adder (KSA). KSA is a parallel prefix form of carry look-ahead adder. It generates the carry signals in $O(log2N)$ time, and is thus widely considered as the fastest adder design possible [13-14].

V.VEDIC MULTIPLIER USING COMPRESSORS

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The compressor adder used in this paper is a

4:2 compressor adder. A lot of research in the past has been carried out on the same [11].

I. 4:2 Compressor Adder

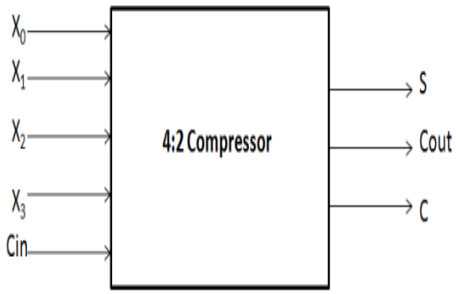


Fig 3.Black box of a 4:2 compressor adder

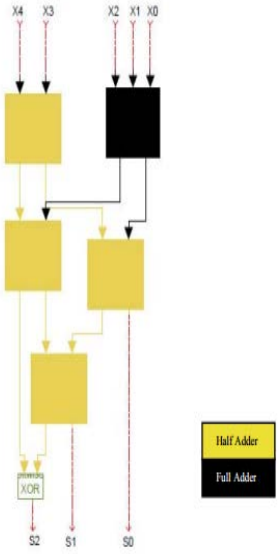


Fig. 4. 4:2 Compressor using full adders and half adders

A 4:2 compressor as shown in Fig.3 is capable of adding 4 bits and one carry, in turn producing a 3 bit output. The internal architecture of the same has been show in fig.4.

II.7:2 Compressor Adder

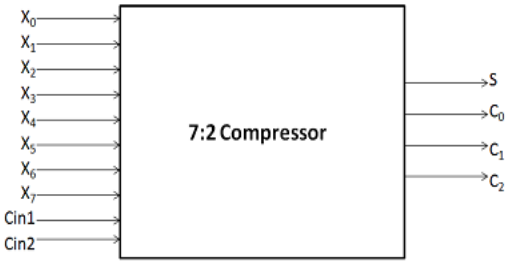


Fig. 5 Black box representation

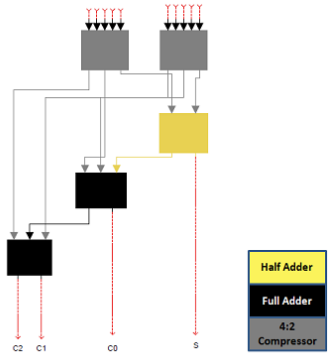


Fig.6 7:2 Compressor using 4:2 Compressor adder of a

7:2 Compressor Adder

Similar to its 4:2 compressor counterpart, the 7:2 compressors as shown in Fig. 5, is capable of adding 7 bits of input and 2 carry's from the previous stages, at a time. In our implementation, we have designed a novel 7:2 compressor utilizing two 4:2 compressors, two full adders and one half adder. The multiplier based on Urdhwa method of multiplication requires several full adders and half adders to add the necessary partial products. This in turn leads to a large propagation delay due to the reasons explained in the previous section. As part of our novel approach, we combined the compressor architectures explained earlier and utilized the same in the Urdhwa based architecture which was formerly. The architecture for the same has been shown below in Fig.7.

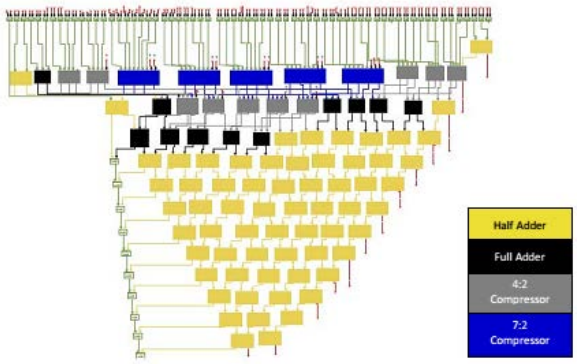


Fig.7 Hardware architecture of Compressor based Urdhwa Multiplier

It can be clearly seen from Fig. 7 that the compressor based Urdhwa multiplier requires only 12 parallel stages as opposed to 15 which was in the case of the conventional Urdhwa Tiryakbhyam multiplier. This is a major improvement with respect to high speed

multiplier design. Also, it can be seen that, many of the stages have now been reduced to a mere logical XOR operation, with an initiative to reduce area.

VI. Simulation Results

I. Sequential FIR Filter

i)Control Unit

The signals from the control unit of sequential FIR filter are explained as shown in fig 8.1.

ii) Data path unit

The operation of data path unit of sequential FIR Filter are explained as shown in the fig 8.2.

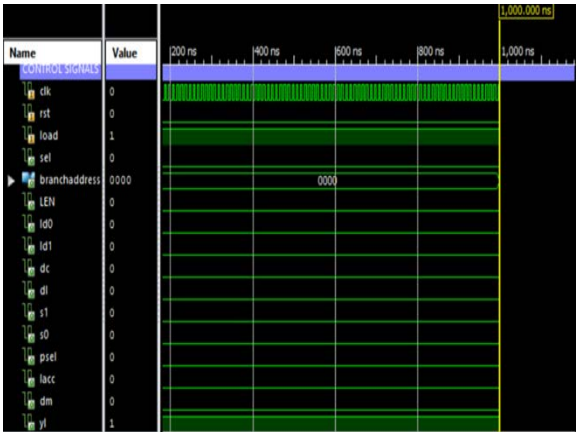


Fig.8.1 Control signals for Sequential FIR Filter

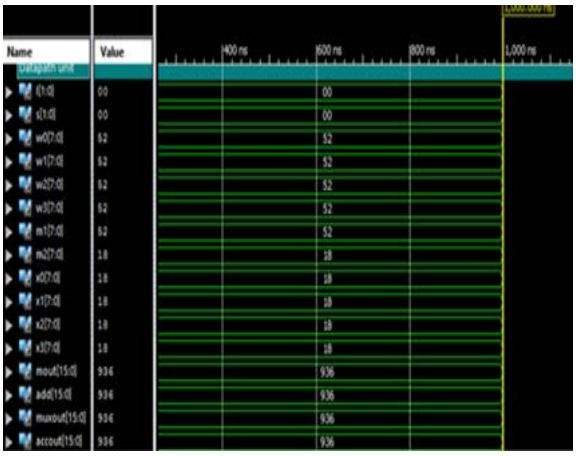


Fig.8.2 Data path unit of Sequential FIR Filter

II. Parallel FIR Filter

i) Control unit

The signals of the control unit of parallel FIR filter are explained as shown in fig 9.1.

ii) Data path unit

The operations of data path unit of sequential FIR Filter are explained as shown in the fig 9.2.

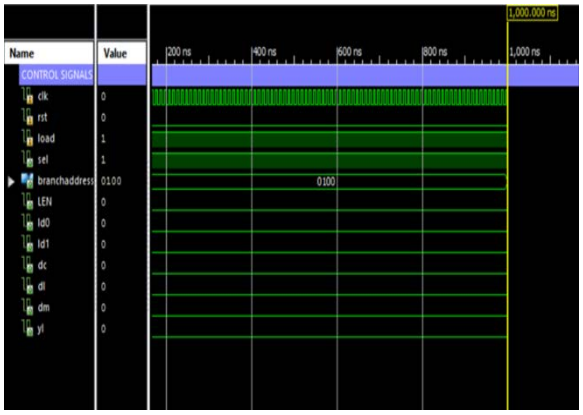


Fig 9.1 Control signals for Parallel FIR Filter

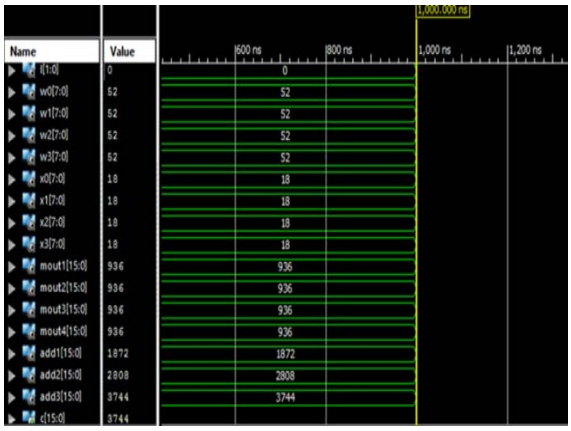
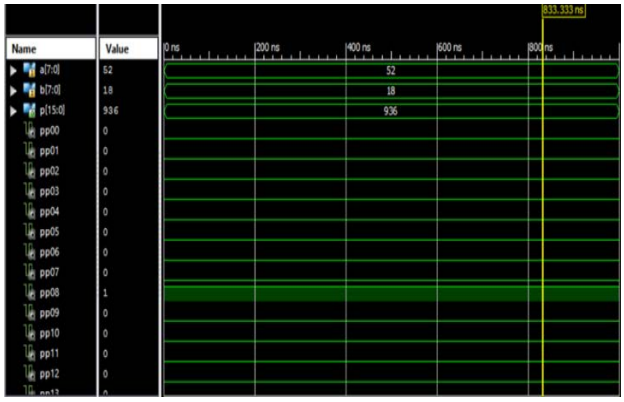


Fig 9.2 Data path unit for Parallel FIR Filter

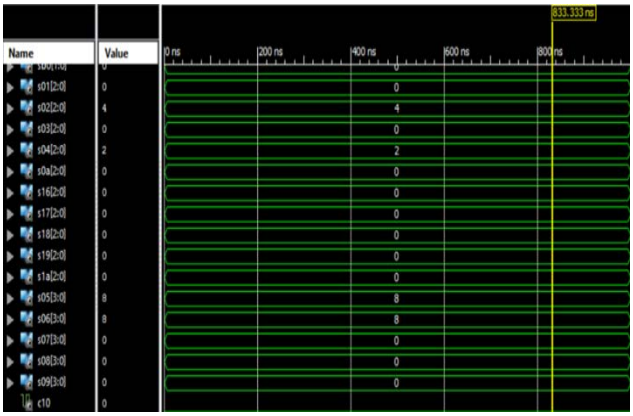
III. Vedic multiplier using Compressor adders

The basic operation of Vedic multiplier using compressors is simulated in Fig 10(a) and 10(b).

Here, inputs are a and b, a= 52, b = 18, p is the output product obtained, p = 936.



(A)



(B)

Fig 10. Vedic multiplier using Compressor adders

VII. Synthesis Results of Parallel and Sequential FIR filters

Table1. Synthesis results of Parallel FIR Filter

S.NO	NAME OF THE MULTIPLIER	AREA (# slices)	DELAY (ns)
1	Wallace tree multiplier using Full adders and Half adders	341	68.5
2	Wallace tree multiplier using Carry skip adder	344	67.7
3	Vedic multiplier using ripple carry adder	430	64
4	Vedic multiplier using Kogge-stone Adder	783	64.3
5	Vedic multiplier using Compressor adders	594	62.8

Table2. Synthesis results of Sequential FIR Filter

S.NO	NAME OF THE MULTIPLIER	AREA	DELAY
1	Wallace tree multiplier using Full adders and half adders	87	28.3
2	Wallace tree multiplier using Carry skip adder	87	27.6
3	Vedic multiplier using Ripple carry adder	109	22
4	Vedic multiplier using Kogge-stone adder	196	24.4
5	Vedic multiplier using Compressor adders	152	20.8

From the results obtained, it can be concluded that Sequential Microprogrammed FIR Filter using Vedic multiplier with compressor adders is faster and requires less area than the existing system.

VIII.CONCLUSION

Digital filters are one of the main elements of DSP. FIR filter which mainly comprises of multiply-accumulate structure is the most commonly used digital filter. Since the performance of FIR Filter mostly depends on the multiplier used, an enhanced and improved multiplier will ameliorate the overall system performance. In this paper, we designed and implemented micro programmed sequential and parallel FIR filter architectures in Xilinx spartan3e FPGA using Wallace tree multiplier/conventional adder, Wallace tree multiplier/Carry skip adder, Vedic multiplier/ripple carry adder, Vedic multiplier/Kogge-Stone adder and Vedic multiplier using compressors combinations respectively.

IX.REFERENCES

1. S. M. Qasim, M. S. BenSaleh and A. M. Obeid, "Efficient FPGA implementation of microprogram control unit based FIR filter using Xilinx and Synopsys tools," *Proc. of Synopsys Users Group Conference (SNUG)*, Silicon Valley, USA, pp. 1-14, March 2012.
2. M. A. Ashour and H. I. Saleh, "An FPGA implementation guide for some different types of serial-parallel multiplier structures," *Microelectronics J.*, Vol. 31, PP. 161-168, 2000.
3. S. M. Qasim, A. A. Telba and A. Y. AlMazroo, "FPGA design and implementation of matrix multiplier architectures for image and signal processing applications," *Int. J. Comp. Sci. Network Security*, Vol. 10, No. 2, pp. 168-176, Feb. 2010.
4. M. Obeid, S. M. Qasim, M. S. BenSaleh, Z. Marrakchi, H. Mehrez, H. Ghariani and M. Abid, "Flexible reconfigurable architecture for DSP applications," *Proc. of 27th IEEE Intl. System-on-Chip Conf. (SOCC),* pp. 204-209, Sept. 2014.
5. S. M. Qasim, M. S. BenSaleh, M. Bahaidarah, H. AlObaisi, T. AlSharif, M. Alzahrani and H. AlOnazi, "Design and FPGA implementation of sequential digital FIR filter using microprogrammed controller," *Proc. of 4th Intl. Congress on Ultra Modern Telecommunications and Control Systems and Workshops (ICUMT),* pp. 1002-1005, Oct. 2012.
6. M. S. BenSaleh, S. M. Qasim, M. Bahaidarah, H. AlObaisi, T. AlSharif, M. Alzahrani and H. AlOnazi, "Field programmable gate array realization of microprogrammed controller based parallel digital FIR filter architecture," *Proc. of World Congress on Engineering and Computer Science (WCECS)*, pp 828–831, Oct. 2012.
7. S. M. Qasim and M. S. BenSaleh, "Hardware implementation of microprogrammed controller

based digital FIR filter," *IAENG Trans. Engg. Tech.*, Vol. 247, pp 29-40, 2014.

8. M. S. BenSaleh, S. M. Qasim, A. A. AlJuffri and A. M. Obeid, "Scalable design of microprogrammed digital FIR filter for sensor processing subsystem," *IEICE Electronic Express*, Vol. 11, No. 14, pp.1-7, Aug. 2014.

9. W. J. Townsend, E. E. Swartzlander and J. A. Abraham, "A comparison of Dadda and Wallace multiplier delays," *Proc*. *SPIE*, Vol. 5205, 2003.

10. A. Aljuffri. M. M. AlNahdi, A. A. Hemaid, O. A. AlShaalan, M. S. BenSaleh, A. M. Obeid and S. M. Qasim, "ASIC realization and performance evaluation of scalable microprogrammed FIR filters using Wallace tree and Vedic multipliers," *Proc. of 15th IEEE Intl. Conf. on Environmental and Electrical Engineering (EEEIC)*, pp.1-4, June 2015, Accepted.

Authors Details:

Pathapati Tanuja, has completed B.Tech in Electronics and Communication Engineering from Panineeya Institute Of Technology and Sciences, affiliated to J.N.T.U Hyderabad in 2013. She is pursuing M.E/M.Tech in Embedded systems and VLSI Design from MVSR Engineering College, affiliated to Osmania University, Telangana, India.

B.Bhavani, is an Assistant Professor in the Department of ECE at MVSR Engineering College, affiliated to Osmania University, Telangana. She has received BE/B.Tech degree in Electronics and Communication Engineering from Andhra University in 2003 and M.Tech in Embedded Systems from J.N.T.U Hyderabad in 2008.