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A LOW POWER 32-BIT MAC UNIT DESIGN USING VEDIC MUTIPLIER AND BRENT-KUNG ADDER

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Abstract

An area-efficient and low-power Multiply Accumulate (MAC) Unit is proposed in this work. The multiplication unit is implemented with vedic multiplier using Urdhava Triyagbhayam Sutra. The Vedic multiplier is used for the multiplication unit so as to reduce partial products and to get high performance and lesser area. The adder unit is implemented using Reversible logic gates. Performance of MAC unit is compared by considering different high performance adders like carry save adder, Kogge-Stone Adder and Brent-Kung Adder for partial product addition in the vedic multiplier. The Vedic Multiplier is designed using Brent Kung Adder that efficiently reduces the area and power consumption compared to other high performance adders. The MAC unit is designed in Verilog HDL; the simulation and synthesis is done in Xilinx 13.2 tool.

Keywords: Vedic Multiplier*, Urdhava Triyagbhayam, Brent Kung adder, Reversible Logic.*

I. Introduction

The multiplication accumulation (MAC) operation is the main computational kernel in Digital Signal Processing (DSP) architectures. With the ever-increasing demand for portable electronic products, an electronic component with low power consumption would surely lead the market trend. Therefore, it is needed to design a less area and low-power MAC unit.

In order to improve the performance of the MAC unit, there are two major bottlenecks that need to be considered. The first one is the partial products reduction network that is used in the multiplication block and the second one is reducing the burden on the accumulator.

The major applications of Multiply-Accumulate (MAC) unit are microprocessors, logic units and digital signal processors, since it determines the speed of the overall system the efficient designs by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are basically executed by insistent application of multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Generally the delay, mainly critical delay, happens due to the long multiplication process and the propagation delay is observed because of parallel adders in the addition stage. The main idea of this paper is to design a high performance Vedic MAC Unit.

II. MAC Unit

Multiplication is the fundamental operation of MAC unit. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers like vedic multiplier in various applications of DSP, networking, etc. The 32 bit MAC unit design is done in two parts; the multiplier unit and the adder unit.

A multiplying function can be carried out in three stages: partial product Generation (PPG), partial product addition (PPA), and final conventional addition (FCA).

In the multiplier unit a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra. The (log2N + 1) partial products are produced by 2N-1 cross products of different widths for N*N. The partial products are generated

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by Urdhava Triyagbhyam Sutra. The adder unit is designed using Reversible logic gates.
The design of MAC architecture consists of 3 sub designs.

- Design of Vedic multiplier.
- Design of adder using reversible DKG gates.
- Design of accumulator which integrates both multiplier and adder stages.

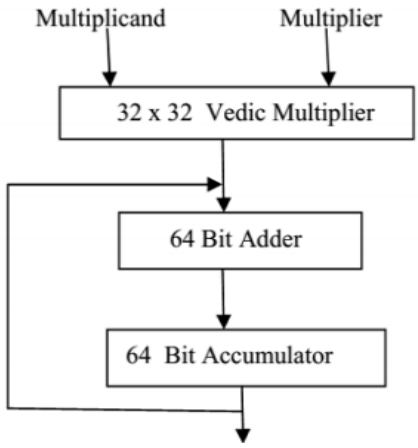


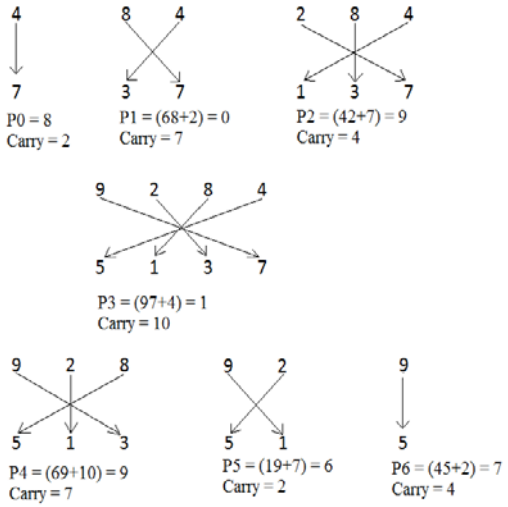
Fig 1: Modified MAC Architecture

III.32 X 32 BIT VEDIC MULTIPLIER

Vedic mathematics is an ancient system of mathematics, which was formulated by Sri Jagadguru Swami Bharati Krishna Tirthaji (1884 - 1960). After a research of eight years, he developed sixteen mathematical formulae from Atharvana Veda. The proposed Vedic multiplier is based on the "Urdhava Triyagbhayam" sutra. These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we will utilize similar techniques to solve the binary number system to make the new aphorism, which will be more compatible for the digital systems.

A.Urdhava Triyagbhayam Sutra

It literally means "Vertically and Crosswise". Shift operation is not necessary because the partial product calculation will perform it in a single step, which in turn saves time and power. This is the main advantage of the Vedic multiplier.
An example for the Urdhva Triyagbhayam sutra is as follows:
9284 * 5137



B. Architecture of Vedic Multiplier

The following fig. 2 shows the design of a 16×16 Vedic multiplier using an 8×8 Vedic multiplier and the design can be implemented using Verilog HDL. Using a 16×16 Vedic multiplier we can design 32 ×32 Vedic multiplier with carry save adder as shown in fig.3. We have modified the final adder stage with the Brent Kung adder.

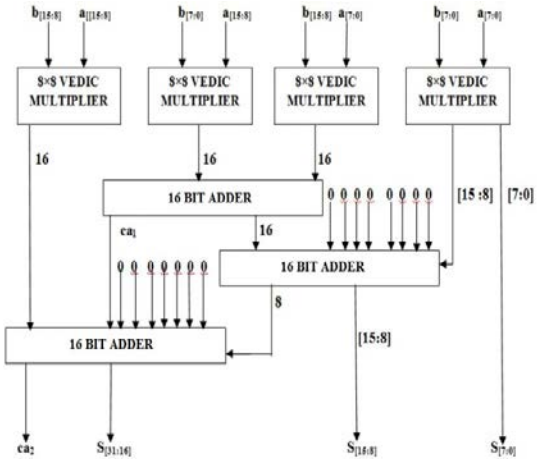


Fig 2: 16×16 Vedic multiplier using 8×8 Vedic multiplier

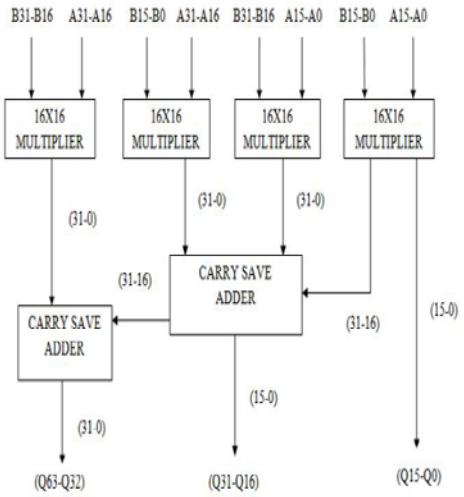


Fig 3: 32 × 32 Vedic Multiplier with Carry save Adder

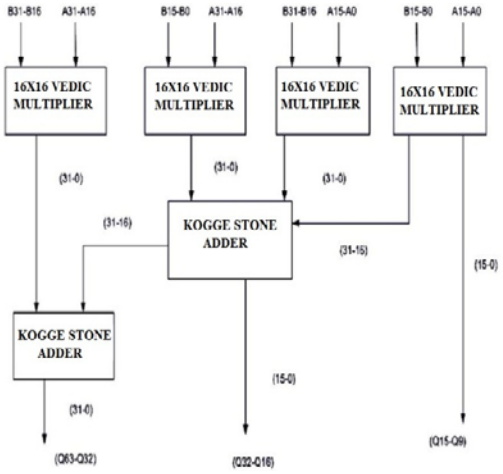


Fig 4: 32 × 32 Vedic Multiplier with Kogge Stone Adder

IV. PROPOSED MODEL

The existing models implement the vedic multiplier using Carry save adder or kogge stone adder for partial product addition. We observed that Kogge Stone Adder gives larger speeds but fails to use minimum area and power. Thus, in order to reduce the area and power we are replacing Kogge stone adder with Brent Kung Adder. The Brent Kung Adder takes lesser no. of black cells and grey cells, thus, reducing the area and power consumption.

A. Brent-Kung Adder

The large number of levels in Brent Kung Adder (BKA) however reduces its operational speed. BKA is also power efficient because of its lowest area delay with large number of input bits.

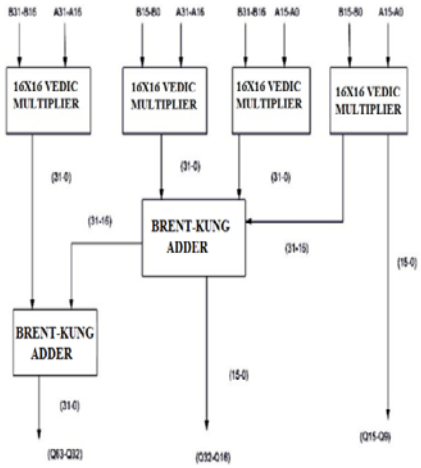


Fig 5: 32 × 32 Vedic Multiplier with Brent Kung Adder

The delay of BKA is equal to (2*log2n)-2. The BKA has the area of (2*n)-2-log2n where n is the number of input bits. The BKA is known for its high logic depth with minimum area characteristics. High logic depth here means high fan-out characteristics.

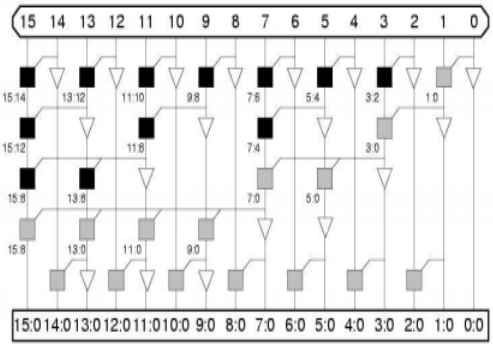


Fig 6: 16-bit Brent-Kung Adder Architecture.

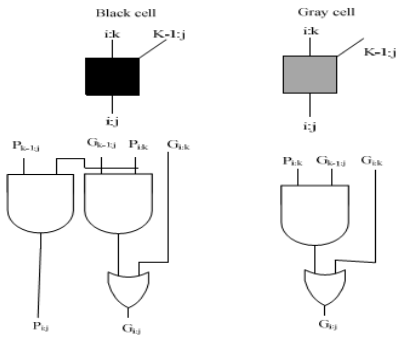


Fig 7: Black cell and Gray cell

B. Design of adder using reversible logic DKG gate

Reversible logic is a unique technique that prevents Loss of information. In this, the numbers of outputs are equal to the number of inputs. A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet showed that a circuit consisting of only reversible gates does not dissipate power. In the design of reversible logic circuits.

1. DKG Gate

A 4* 4 reversible DKG gate that can work singly as a reversible full adder and a reversible full subtractor is shown below. If input A=0, the DKG gate works as a reversible Full adder, and if input A=1 then it works as a reversible Full subtractor. It has been verified that a reversible full-adder circuit requires at least two or three garbage outputs to make the output combinations unique.

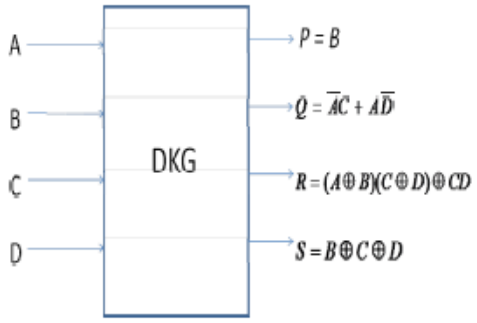


Fig 8a: DKG gate

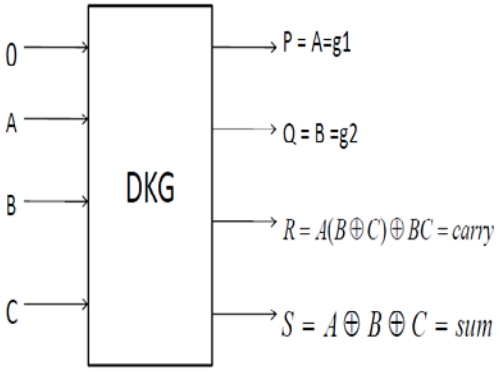


Fig 8b: DKG gate as a Full adder

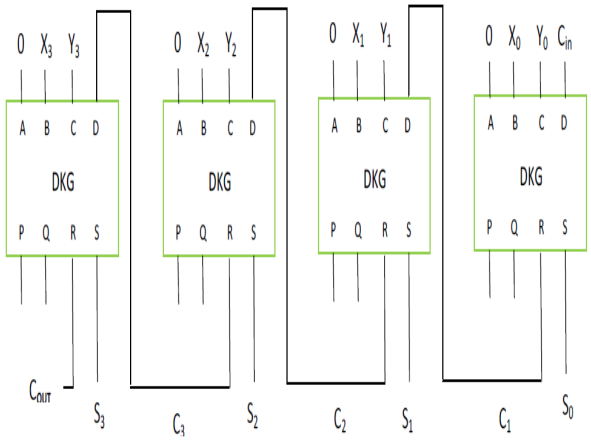


Fig 8c: Parallel adder using DKG gate

C. Accumulator Stage

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using our design had better performance

V. RESULT AND DISCUSSION

The vedic multiplier using the Brent Kung Adder achieves lesser area and lesser power consumption. The area is reduced by 8% while the power is reduced by nearly 50%. The power delay product of the proposed design is also reduced nearly by 48% compared to existing model making it an efficient design.

The design of 32 bit MAC is done in Xilinx. The synthesis is performed out in Xilinx 13.2. The above design is implemented in Verilog Code. Comparison of area, speed and power are tabulated in table below.

Fig 9: Vedic Multiplier Simulation Results

Fig 10: Adder Simulation Results

Fig 10: Multiply and Accumulate unit simulation Results.

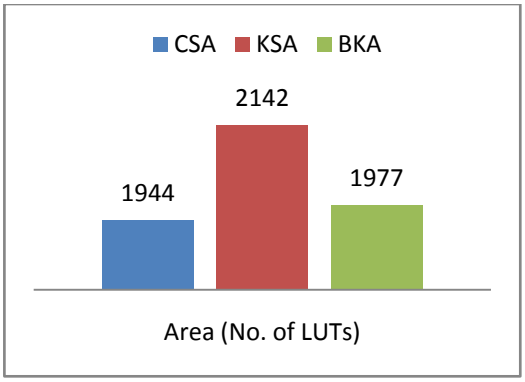


Fig 11: Area Comparison of Vedic MAC Designs using different adders

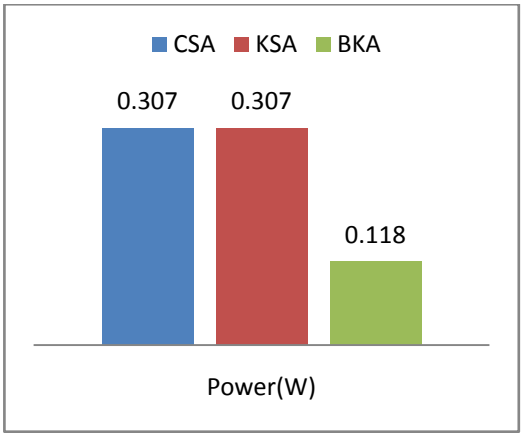


Fig 12: Power Comparison of Vedic MAC Designs using different adders

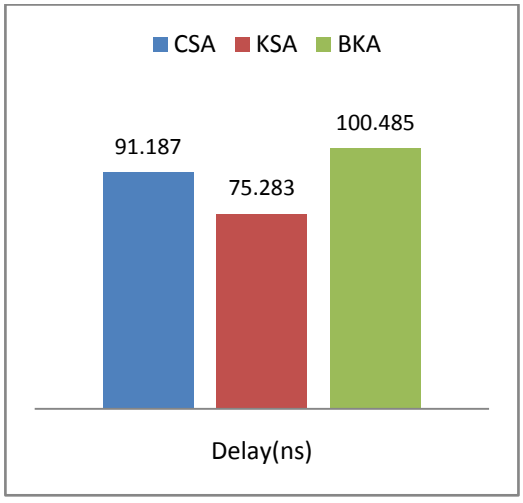


Fig 13: Delay Comparison of Vedic MAC Designs using different adders

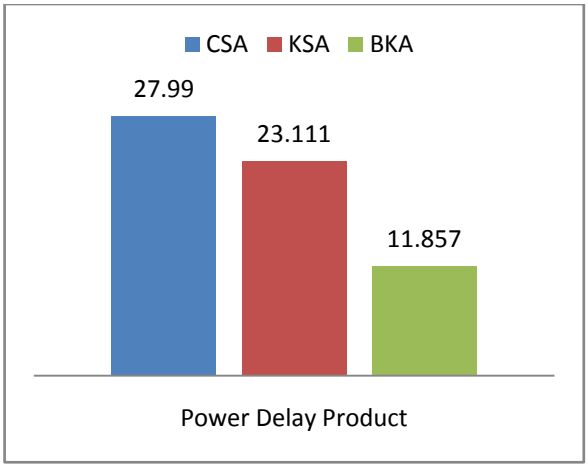


Fig 15: Power Delay Product Comparison of Vedic MAC Designs using different adders

Table 1: Comparison Between different Vedic MAC Performances.

	Using CSA	Using KSA	Using BKA
Device Utilization			
No. of Slices used	1944	2142	1977
Timing			
Delay(ns)	91.187	75.283	100.485
Power Analysis			
Total power(W)	0.307	0.307	0.118
PDP(nJ)	27.99	23.111	11.857

VI. CONCLUSION AND FUTURE WORK

The results obtained by the design of Vedic multiplier with 32 bits and reversible logic are quite good. The work presented is based on 32 – bit MAC unit with Vedic Multipliers. We have designed MAC unit basic building blocks and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyagbhayam sutra with 32-bit Multiplier and reversible logic is the best in all aspects like speed, delay, area and complexity as compared to other architectures.

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