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# A Radiation-Hardened AMBA Bus

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**Abstract**

It designed to meet the command- and data-handling requirements for missions requiring true space-grade radiation hardness and fault tolerance. The design uses parts with total-ionizing-dose tolerance appropriate for deployment on long-term missions in MEO or GEO environments. The design uses a space-quality dual-core processor ASIC, a field-programmable gate array (FPGA), memories, and interfaces to meet the command- and data handling requirements of medium-sized missions. Today's system-on--chip (SOC) is designed with reusable intellectual property cores to meet short time to market requirements. This on-chip bus protocol is differentiated from other on-chip bus protocols with feature of efficient block data transfer. Embedded systems design focuses on low Power dissipation and system-on-chips. A reliable on-chip communication standard is a must in any SOC. The ARM Advanced Microcontroller Bus Architecture (AMBA) is an open-standard, on-chip interconnects specification for the connection and management of functional blocks in system-on a-chip (SoC) designs. It facilitates development of multi-processor designs with large numbers of controllers and peripherals.

***Keywords**:* AMBA,AHB,Difference of buses,radition hardened

## I. Introduction

It is a custom design intended to function as the payload processor for a set of instruments in medium Earth orbit (MEO) and geosynchronous Earth orbit (GEO) applications. These instrument systems often consist of a suite of sensor boards connected through a backplane to a processor board. The processor board is responsible for configuring the sensor boards, reading data from the sensor boards, and sending that data in a packaged format to the space-vehicle host.

Traditional bus protocols like the advanced microcontroller bus architecture (AMBA) advanced high-performance bus (AHB) and advanced eXtensible interface (AXI) from ARM Holdings, Wishbone from Silicore Corporation,

Open Core Protocol (OCP) from OCP International Partnership and CoreConnect from IBM are commonly used in industry. The main characteristic of all these buses is that they transfer data linearly.The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on chip communications standard for designing high-performance embedded microcontrollers. Three distinct buses are defined within the AMBA specification.

- Advanced High-performance Bus (AHB)
- Advanced System Bus (ASB)
- Advanced Peripheral Bus (APB)

A test methodology is included with the AMBA specification which provides an infrastructure for modular macrocell test and diagnostic access.

**i**. Advanced High-performance Bus (AHB): The AMBA AHB is for high performance, high clock frequency system modules. The AHB acts as the high performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macrocell functions. AHB is also specified to ensure ease of use in an efficient design flow using synthesis and automated test techniques.

**ii.** Advanced System Bus (ASB): The AMBA ASB is for high-performance system modules. AMBA ASB is an alternative system bus suitable for use where the highperformance features of AHB are not required. ASB also supports the efficient connection of



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processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macro cell functions.

**iii.** Advanced Peripheral Bus (APB): The AMBA APB is for low-power peripherals. AMBA APB is optimized for minimal power consumption and reduced interface complexity to support peripheral functions. APB can be used in conjunction with either version of the system bus.

## II. ARCHITECTURE

Its architecture is based on a processor application-specific integrated circuit (ASIC) that is supported by external static random-access memory (SRAM), non-volatile memory, a field-programmable gate array (FPGA), and board-level physical layer interfaces.

It can communicate directly with a host space vehicle over both MIL-STD-1553B and Space Wire interfaces. To meet standards it must also support serial interfaces on its backplane connectors. The serial interfaces include I2C and multi-gigabit Ser Des-based protocols. The design also supports discrete I/O interfaces that can be connected to other boards. on the backplane or to the space vehicle. The SBC accepts space-vehicle clocks that can be used for system timing. It is based on 180 nm technology.
The processor ASIC executes flight software and is at the top of the command- and data-handling control hierarchy. The processor occupies the top level of control for this board. It boots from code stored in the external non-volatile memories, transfers flight software to SRAM, and then begins execution of flight software from SRAM.

The processor ASIC has built-in hardware support for SpaceWire, error detection and correction (EDAC) on external memories.

The FPGA provides a platform for custom hardware co-processing functions to reduce the load on the processor ASIC. The FPGA also has built-in physical layer support for high-speed serial, LVDS, I2C, and JTAG (Joint Test Action Group) interfaces. These capabilities are hard IP blocks instantiated in the FPGA that can be accessed by soft designs in the user fabric

## III. AMBA-BASED MICROCONTROLLER

An AMBA-based microcontroller shown in Figure 1 typically consists of a high-performance system backbone bus (AMBA AHB or AMBA ASB), able to sustain external memory band width, on which the CPU, on-chip memory and other Direct Memory Access (DMA) devices reside. This bus provides a high bandwidth interface between that are involved in the majority of transfers. Also located on the high performance bus is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located.

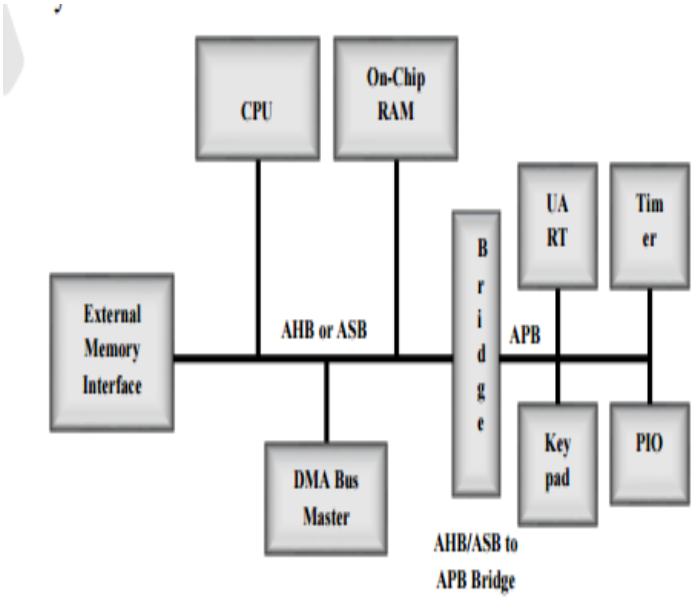


**Figure 1: AMBA based microcontroller**

## IV. POWER

**Beginning Timing Optimizations**

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| ELAPSED TIME | AREA | WORST NEG SLACK | TOTAL SETUP COST | DESIGN RULE COST | ENDPOINT | LEAKAGE POWER |
|---|---|---|---|---|---|---|
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| Global Optimization (Phase 31) | | | | | | |
| Global Optimization (Phase 32) | | | | | | |
| Global Optimization (Phase 33) | | | | | | |
| Global Optimization (Phase 34) | | | | | | |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |

**Beginning Delay Optimization**

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| | | | | | | |
|---|---|---|---|---|---|---|
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
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| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
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| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
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| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
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| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |
| 0:00:03 | 101793.8 | 0.00 | 0.0 | 0.0 | | 50329944.0000 |

### III. ADVANCED HIGH-PERFORMANCE BUS (AHB)

AHB is a new generation of AMBA bus which is intended to address the requirements of highperformance synthesizable designs. It is a high performance system bus that supports multiple bus masters and provides high bandwidth operation. AMBA AHB implements the features required for high performance, high clock frequency systems including:

- Burst transfers
- Split transactions
- Single-cycle bus master handover
- Single-clock edge operation
- Non-tristate implementation
- Wider data bus configurations (64/128 bits)

Bridging between this higher level of bus and the current ASB/APB can be done efficiently to ensure that any existing designs can be easily integrated. An AMBA AHB design may contain one or more bus masters, typically a system would contain at least the processor and test interface. However, it would also be common for a Direct Memory Access (DMA) or Digital Signal Processor (DSP) to be included as bus masters. The external memory interface, APB Bridge and any internal memory are the most common AHB slaves. Any other peripheral in the system could also be included as an AHB slave. However, low-bandwidth peripherals typically reside on APB.

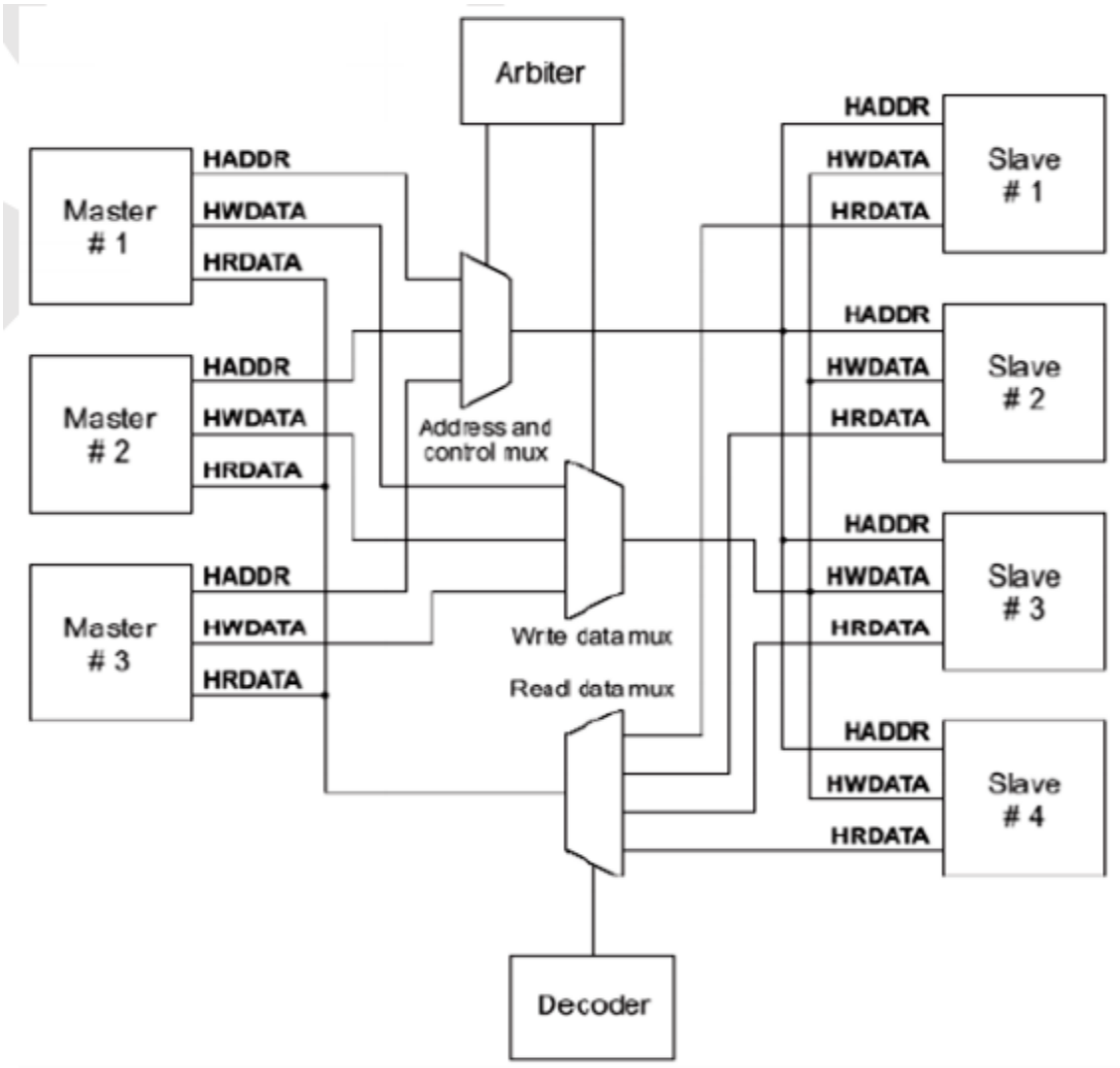


**Figure 2: AMBA AHB Block diagram**

A typical AMBA AHB system design contains the following components:

1. **AHB Master:** A bus master is able to initiate read and write operations by providing an address and control information. Only one bus master is allowed to actively use the bus at any one time.

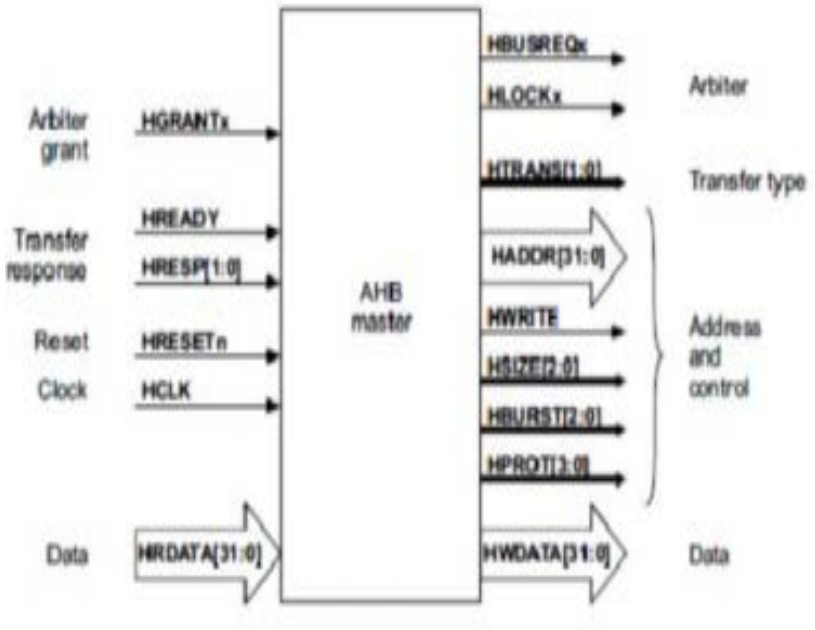


**Figure 3: AHB bus master Interface**

**2. AHB Slave**: A bus slave responds to a read or write operation within a given address-space range. The bus slave signals back to the active master the success, failure or waiting of the data transfer.

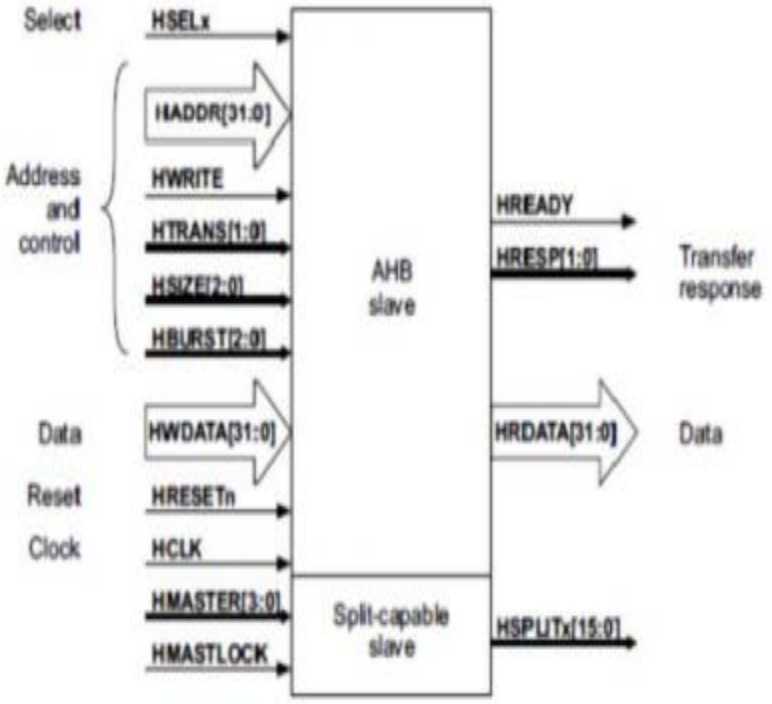


**Figure 4: AHB bus slave Interface**

**3. AHB Arbiter:** The bus arbiter ensures that only one bus master at a time is allowed to initiate data transfers. Even though the arbitration protocol is fixed, any arbitration algorithm, such as highest priority or fair access can be implemented depending on the application requirements. An AHB would include only one arbiter, although this would be trivial in single bus master.

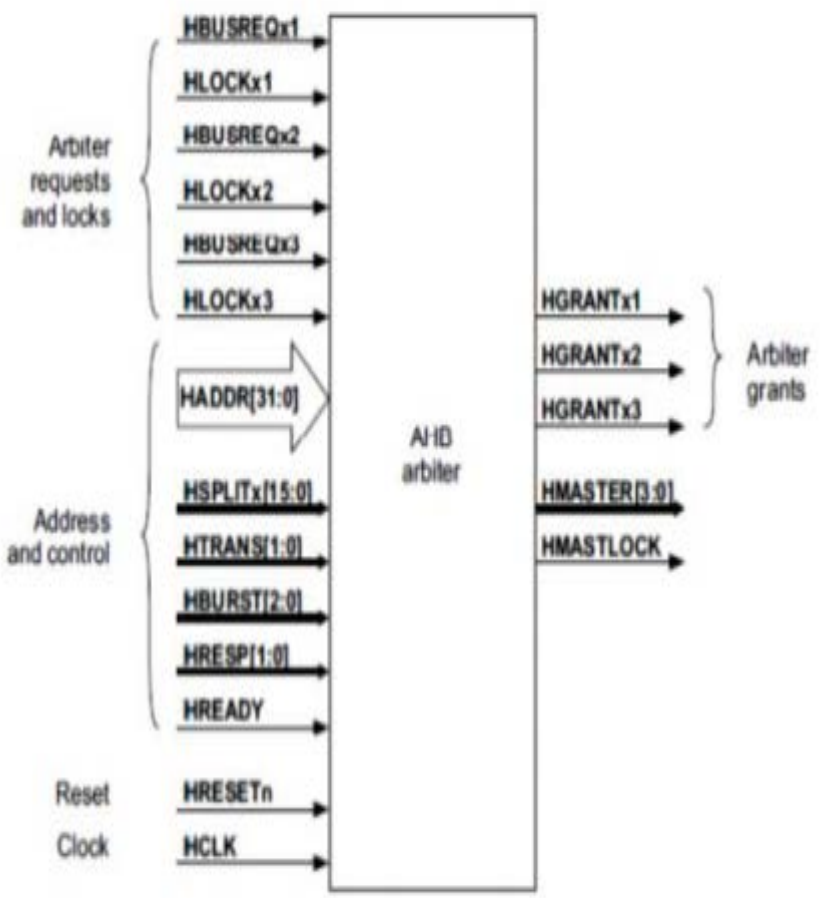


**Figure 5: AHB arbiter interface**

**4. AHB Decoder**: The AHB decoder is used to decode the address of each transfer and provide a select signal for the slave that is involved in the transfer. A single centralized decoder is required in all AHB implementations.

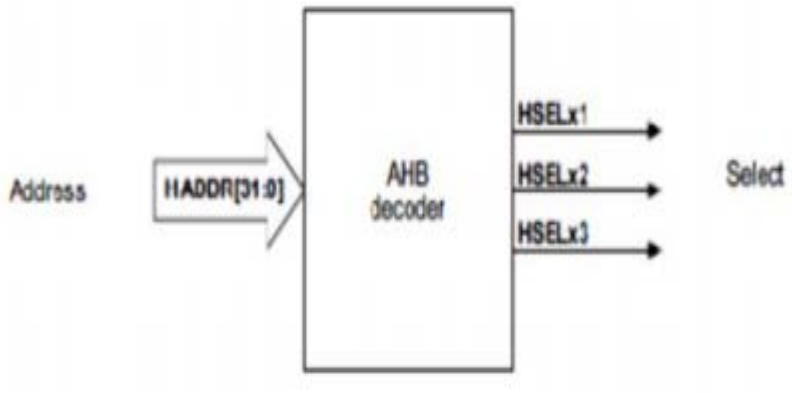


**Figure 6: AHB decoder interface**

**AMBA Signal Names**

•All AMBA signals are named such that the first letter of the name indicates which bus the signal is associated with.

• A lower case n in the signal name indicates that the signal is active LOW, otherwise signal names are always all upper case.

• Test signals have a prefix T regardless of the bus type AHB signal prefixes-H indicates an AHB signal. For example, HREADY is the signal used to indicate that the data portion of an AHB transfer can complete. It is active HIGH.

•APB signal prefixes-P indicates an APB signal. For example, PCLK is the main clock used by the APB.

***Choice of Bus***

Before deciding on which bus or buses should use in system should consider the following:

• Choice of system bus

• System bus and peripheral bus

• When to use AMBA AHB/ASB or APB

Choice of system bus-Both AMBA AHB and ASB are available for use as the main system bus. Typically the choice of system bus will depend on the interface provided by the system modules required The AHB is recommended for all new designs, not only because it provides a higher bandwidth solution, but also because the singleclock-edge protocol results in a smoother integration with design automation tools used during a typical ASIC development. System bus and peripheral busBuilding all peripherals as fully functional AHB or ASB modules is feasible but may not always be desirable:

• In designs with a large number of peripheral macrocells the increased bus loading may increase power dissipation and sacrifice performance.

•Where timing analysis is required, the slowest element on the bus will limit the maximum performance.

• Many simple peripheral macrocells need latched addresses and control signals as opposed to the high-bandwidth macrocells which benefit from pipelined signalling.

• Many peripheral functions simply require aselection strobe which conveys macrocell selection and read/write bus operation, without the requirement to broadcast the high-frequency clock signal to every peripheral.

When to use AMBA AHB/ASB or APB- A full AHB or ASB interface is used for:

• Bus masters On-chip memory blocks

• External memory interfaces

• High-bandwidth peripherals with FIFO interfaces

• DMA slave peripherals

• A simple APB interface is recommended for:

• Simple register-mapped slave devices

• Very low power interfaces where clocks cannot be globally routed

• Grouping narrow-bus peripherals to avoid loading the system bus.

**IV. CONCLUSION**

It a low-cost, low-power payload processor board that is suitable for use on medium-sized missions. With its floating-point support and multi-core architecture, it can be used as for command and data handling, processing of mission data, or both.

Carrying out literature review is very significant in any research project. It clearly establishes the need of the work and the background development. It generates related queries regarding improvements in the study already done and allows unsolved problems to emerge and thus clearly define all boundaries regarding the development of the research work. This paper reviews the bus architectures of radiation hardened AMBA 2.0

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