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Design of Four Port Router for Network on Chip Using VERILOG

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Abstract

Multiprocessor system on chip (SOC) has emerged as a new trend for system on chip design but the wire and power design constraints are forcing to adopt new designs methodologies. Researchers has pursued a solutions to this problem i.e. Network on Chip (NOC). Network on chip is a communication system on an integrated circuits, typically between intellectual property (IP) cores in a system on a chip.[1] Network on chip architecture better supports the integration of SOC consists of on chip packet switched networks. We has developed a Router a packet based protocol. In this Router we have taken functionality references from an actual Router the design is being implemented on single chip using Verilog code.

Keywords: FIFO, FSM, Network-On-Chip, Register Blocks, and Router Simulation.

1. Introduction

System on chip (SOC) is a complex interconnection of various kind of functional element which creates communication bottleneck in the gigabit communication due to its bus based architecture. There was thus need of system that explicit modularity and parallelism both, hence network on chip possesses many such attractive properties and solves many problems occurred at bottleneck communication.[2] This communication on network on chip is carried out by router and thus for a better implementation of NOC a router should be efficiently designed.

A **router** is a networking device that forwards data packets between computer networks. A router is connected to two or more than transmitted data lines of different network (opposed to a network switch, which connects data lines from one single network). When the required data packet comes in on one of the lines, the router reads the address information in the form of a packet to determine its final destination. It is a device that drives the incoming packets which comes from the input to the output channel based on the address field contained in the packet header. Router has one input port from where the packet enters and three output ports from where the output is driven.[3] The router here has an active low synchronous input reset_n it resets a router with an active high clocking event, under reset condition the router FIFOs are made empty and the valid out signals goes low indicating that no valid packet is detected on the output data bus. This helps to understand how router is controlling the signal from source server network to the destination client network based on the header address. This idea is borrowed from wide area network and large scale multiprocessor routers based network. It tells when a data have to be extracted for a particular port and also gives the idea whether a port is full or empty. This method removes most of the problem and also improves the performance of the router. Other than packet routing it also includes features such as parity checking, it is a kind of an error detecting technique which tests the integrity of digital data those are transmitted between server and client.[4] This technique ensures that the data transmitted by the server network is received by the client network without getting corrupted. Sending packets that refer router input protocol and reading packet refer router output protocol.

Other than using routers at home or small office to simply pass data, may also be used to connect two or more logical groups of computer devices generally known as subnets, each with a different sub-network address.

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WHY WOULD I NEED A ROUTER?

For most home users, they may want to setup LAN (local area network) or a WLAN(wireless LAN) and connect all computers to the Internet without paying a full broadband subscription services to their ISP for each computer on the network. In many instances, an ISP allows you to use a router and connect multiple computers to a single Internet connection and pay a less fee for each more additional computer sharing the connection.[5] This is when home users will want to look at smaller routers, called as broadband routers that enables two or more computers to share an Internet connection. Within a business or organization, you might need to connect multiple computers to the Internet, but also want to connect multiple private networks not all routers are being created as equal since their jobs will differ slightly from network to network.

What defines a router is not its color, shape, size or manufacturer, but its function of routing packets of data between computers. A cable modem, which routes the data between a PC and an ISP can be considered as a router.

Broadband or ICS routers will look a little different depending on the manufacturers, but wired routers are like generally a small box shape hardware devices with ports on the front or at the back into which you plug each of the computers, along with a port to plug-in the broadband modem. These connection ports will allow the router to do its functionality of routing the data packets between the computers and the data going to and from the Internet.[6] Depending on the type of Internet connection and modem you have, you could also choose a router with phone or fax machine ports.

ROUTER DESIGN PRINCIPLES

This document provides specifications for the Router is a packet based protocol. Router is a device which forward the given data packets among computer networks. It is an OSI layer 3 routing devices. It drives an incoming packet to an output channel generally based on the address fields contained in the packet header. Router packet the packet consists of 3 parts: header, parity and payload each of 8 bit width and the length of the payload can be extended between 3 between 1 byte to 63 byte.

Header packet contains two fields DA and length, destination address of the packet is of 2 bits. Router drives the packet to the respective port based on this destination address of the packets. Each of the output port, has 2-bit unique port address. If the destination address of the packet matches the port address, then router drives the data packets to the output port given address „3" is invalid. Length of data is 6-bits which specify the number of the data bytes. A particular packet can have a minimum data size of 1 byte and a maximum size of 63 bytes.[7] Payload is the data information send. Data should always be in terms of the bytes.

Parity field contains the security check of the data packets send calculated as bitwise parity over the header and payload bytes of the packets.

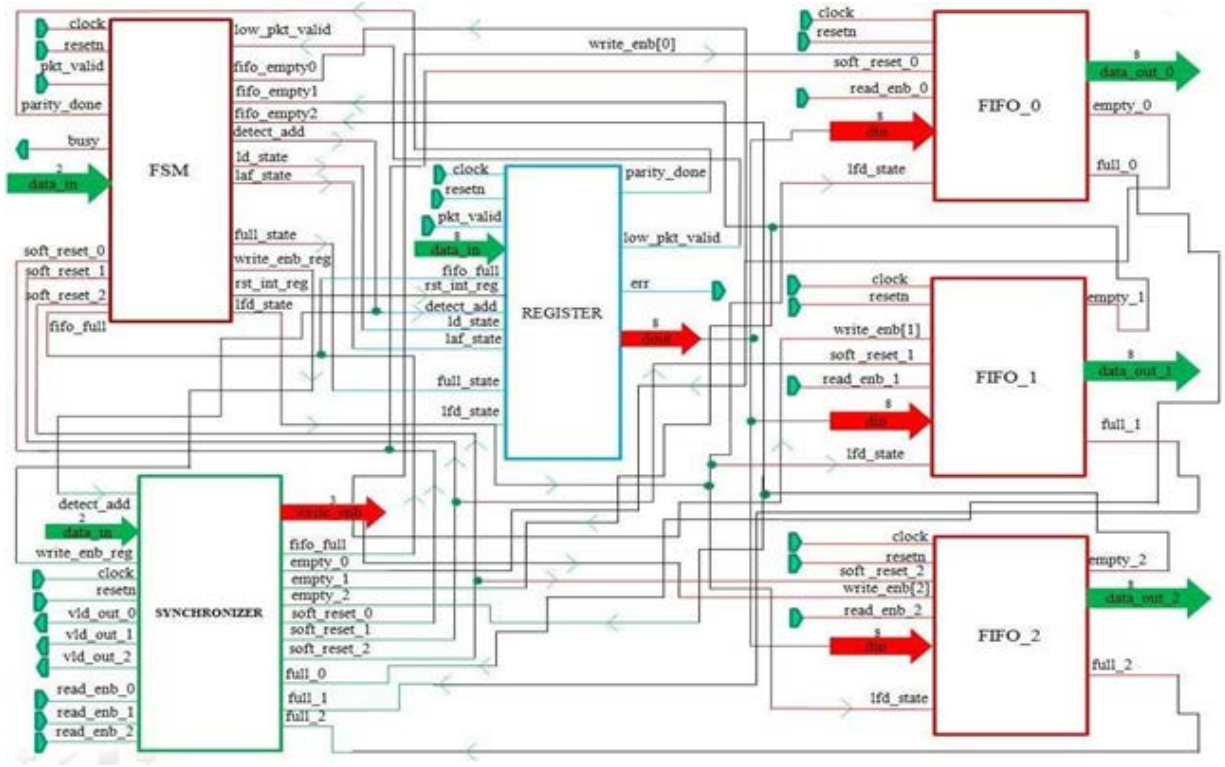
This router supports three parallel connections at the same given time it uses store and forward of flow control and FSM Controller routing which improves the performance of router. This store and forward mechanism is best as it does not reserve channels and thus does not lead to idle physical channels.

Router has been a synchronous protocol. Clock signal controls when data can change and when it is valid for reading. The data rate will change with the change in the clock rate. As compared with its counterpart I2C, ROUTER is suited more for data stream application communication between IP"s.

OPERATION

The Four Port Router Design is done by using of the four blocks. The blocks are 8-bit register, synchronizer, router controller and output block. The controller block is design by using FSM design and the output block consists of three FIFO"s that are combined together. The FIFO"s stores the data packets and at times when you want to send data, the data will be read from the FIFO"s. This design has three outputs i.e. 8-bit size and one 8-bit data input port it is basically used to drive the data into router. We are using the clock which is globally, reset signals, error signal and busy signals are the outputs of the router. The FSM controller gives the busy signal and the register gives the busy signals. Synchronizer provides synchronization between the router FSM and the router FIFO modules it provide a faithful communication between the single input port and three output ports. Register module implement four

internal registers in the order to hold a header byte, FIFO full state byte, packet parity byte and internal parity. All the registers in this module are latched on the rising edge of the clock. [8]



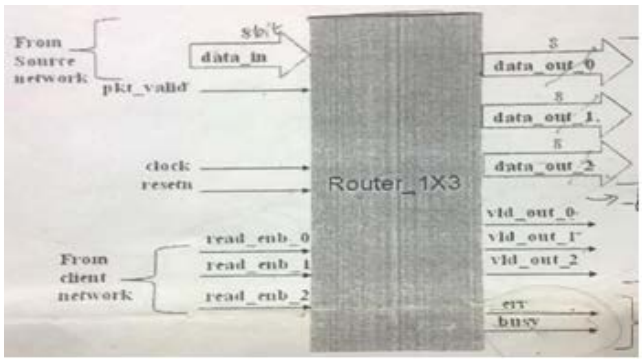


Figure 1: Block diagram of Router_1X3

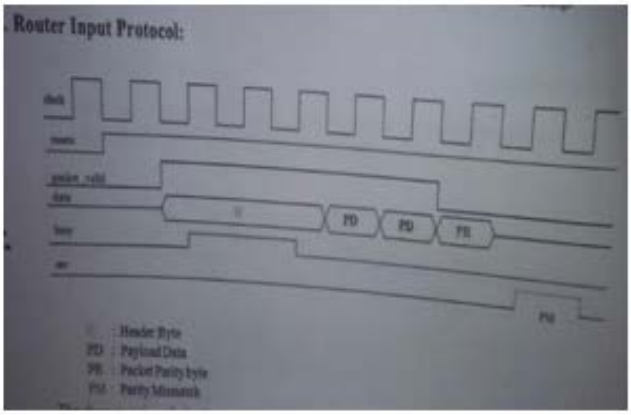


Figure 2: Router_Input_Protocol

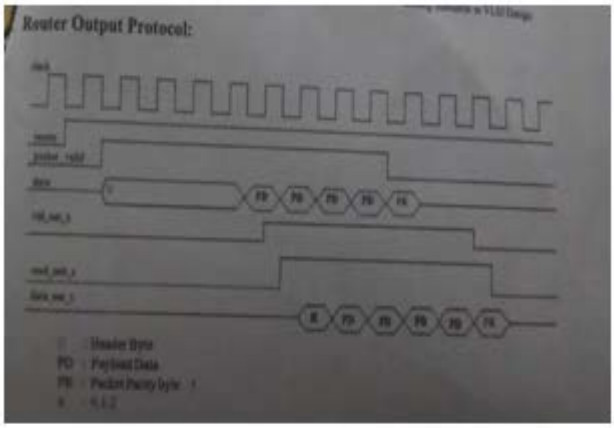


Figure 3: Router_Output_Protocol

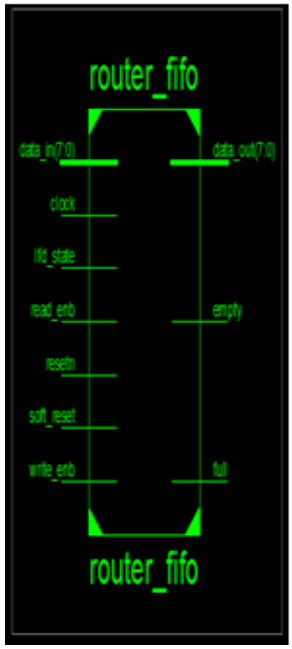


Figure 4: Router_FIFO

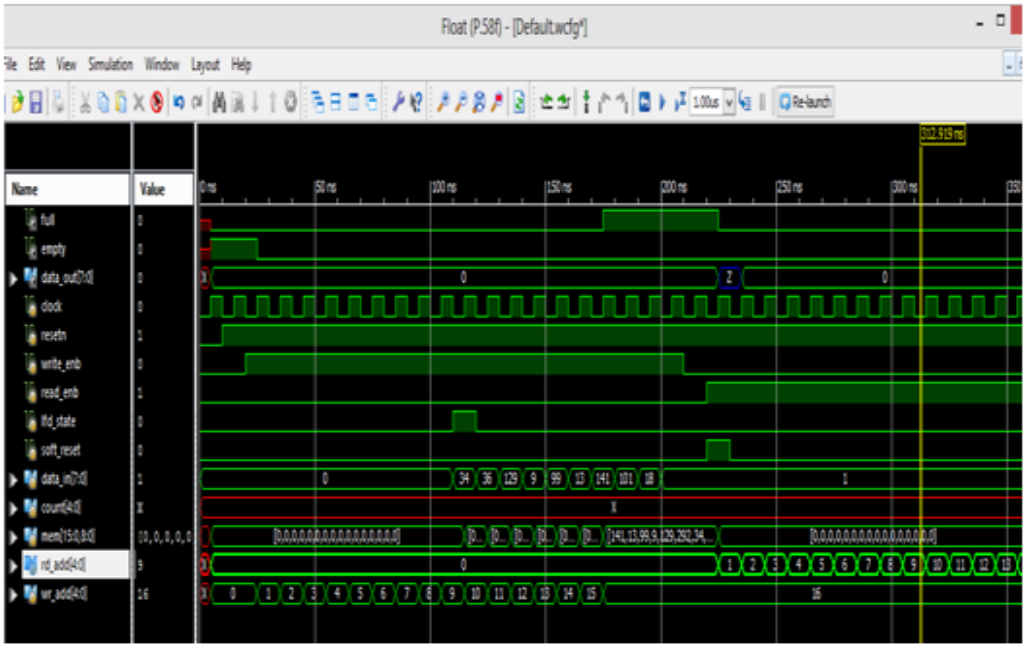


Figure 5: FIFO_simulation

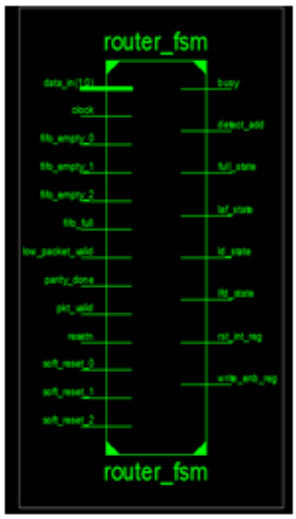


Figure 6: Router_FSM

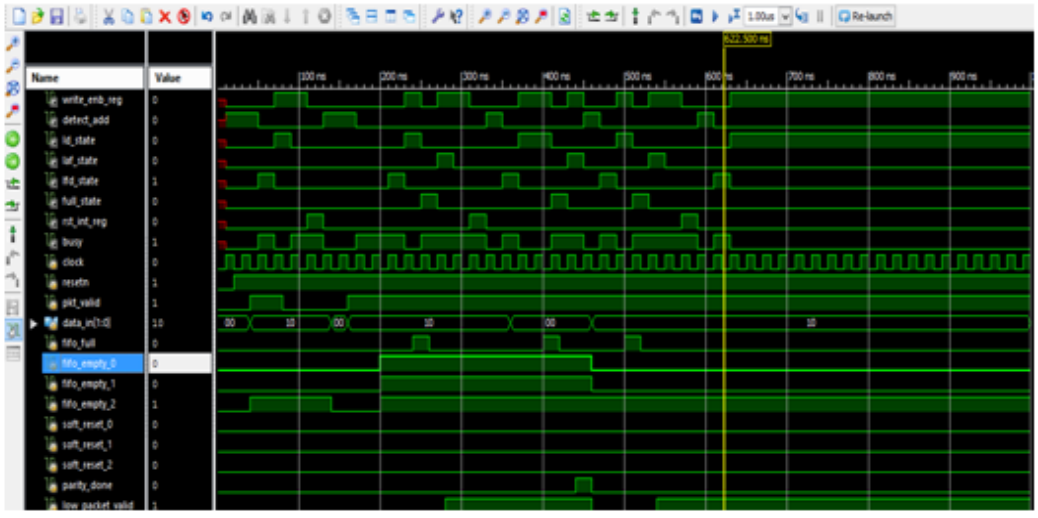


Figure 7: FSM_simulation

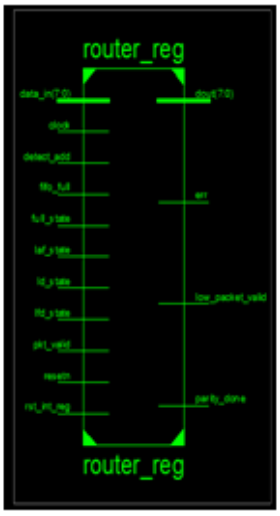


Figure 8: Router_reg

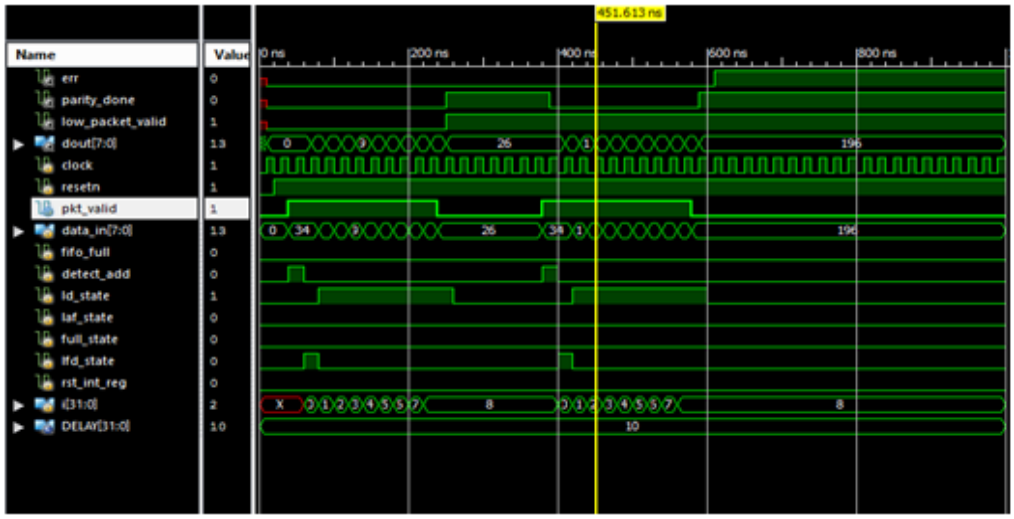


Figure 9: reg_simulation

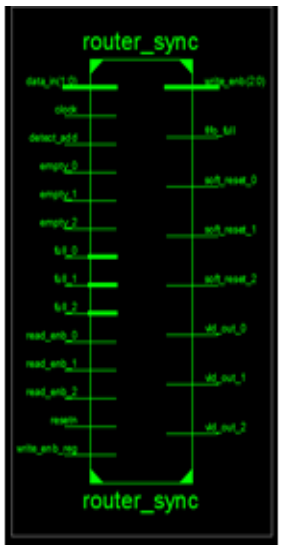


Figure 10: Router_sync

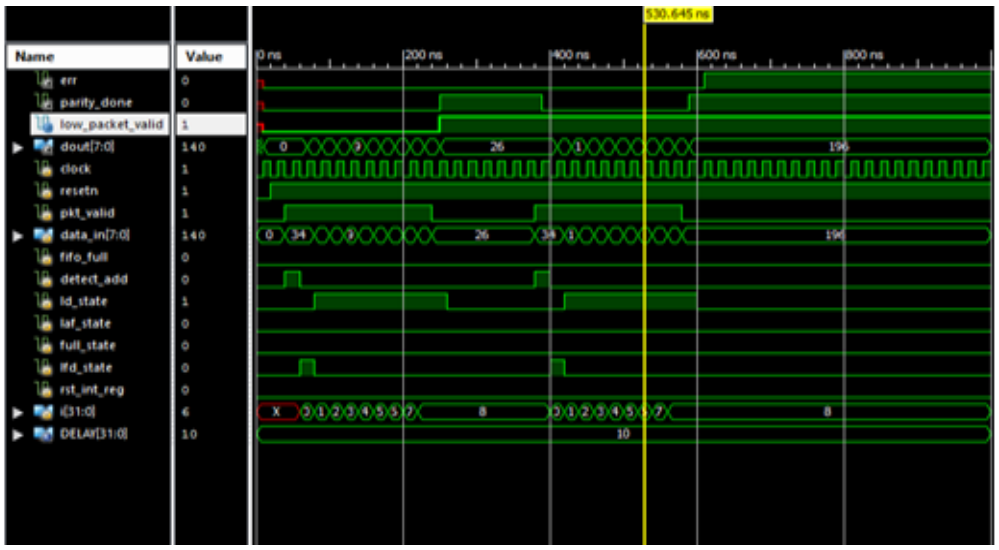


Figure 11: sync_simulation

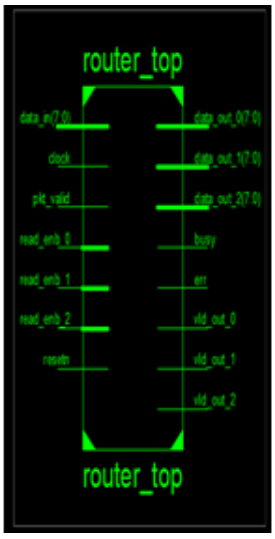


Figure 12: Router_top

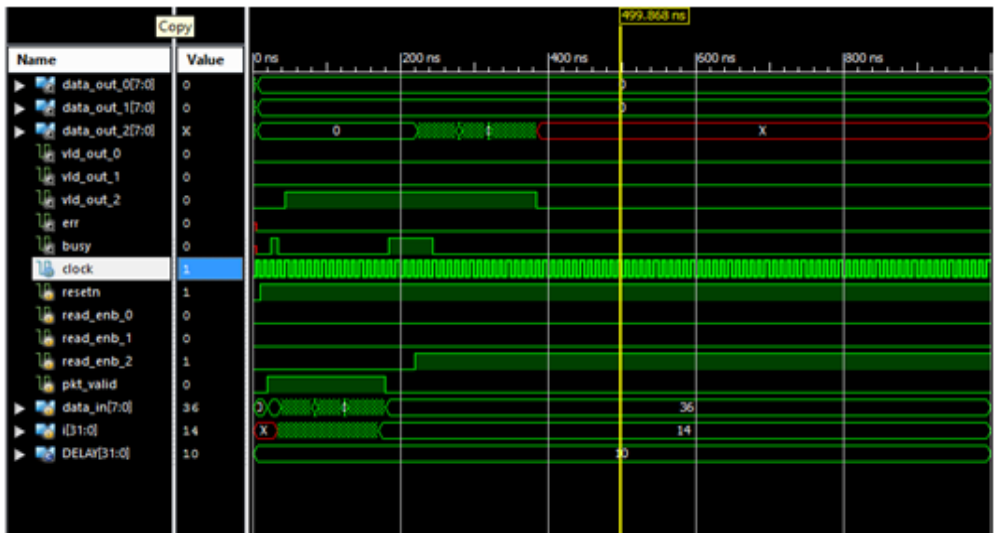


Figure 13: top_simulation

CONCLUSIONS

The proposed design of 1*3 Router is simulated and synthesized in Xilinx ISE 14.2 tool and the proper code is being written in Verilog. This proposed design has high speed and less delay.

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