ISSN: 2456-043X

IJESAR

International Journal of Engineering Science and Generic Research (IJESAR)
Available Online at www.ijesar.in
Volume 2; Issue 3; May-June-2016; Page No. 60-67

Yield Enhancement Techniques of VLSI Technology

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Abstract

Several yield Enhancement techniques have been proposed for the last two stages of fabrication. Our approach is based on the ability to improve the yield during integrated circuit fabrication through defect detection and defect reduction. In this paper we have classified the defects on lithography layer of the wafer and then reduced them so as to enhance the yield of an integrated circuit. This is done by optimizing the inspection recipe parameter on defect capture rate. It is possible to improve the yield of an integrated circuit by minimizing the number of defects on it. During the fabrication of an integrated circuit on the wafer there are many steps like lithography, etching, oxidation, deposition, CMP etc through which a single wafer has to go many times, In this whole procedure of fabrication certain particle my fall on wafer or may result in scratches on wafer .These type of defects result in yield loss and may lead to the failure of integrated circuit.

Keywords: Wafer, Defects, integrated circuits, Lithography, threshold, focus offset, recipe, defect inspection tool, ORS.

INTRODUCTION

Yield is defined as the ratio of the number of products that can be sold to the number of products that can be manufactured. In semiconductor industry yield is represented by the functionality and reliability of integrated circuit produced on the wafer surface. During the manufacturing of integrated circuit yield loss is caused for example by defects, faults, process variation and design .During processes as ion implantation, deposition, etching ,planarization and cleaning etc failure responsible for yield loss are observed. Several examples of contaminations and mechanisms responsible for yield loss are listed in the following: a) Airborne Molecular Contamination (AMC) or particles of organic or inorganic matter caused by the environment or by the tools; b) process induced defects as scratches, cracks, and particles, overlay faults, and stress; c) process variations resulting, e.g., in differing doping profiles or layer thicknesses; d) the deviation from design, due to pattern transfer from the mask to the wafer, results in deviations and variations of layout and critical dimensions; and e) diffusion of atoms through layers and in the semiconductor bulk material[1],[2].

2. Classification of defects on lithography layer

Defect on lithography layer can be as extra or missing material in the IC structure and are referred to as spot defects. Spot defects can occur in any of the conducting, semiconducting or insulating layers of the IC and may lead to alteration in the topography of intended circuit. Defect can be scratches on a wafer during mis-handling. Defect can be any particle on the wafer which may or may not harm the IC. Contamination or unwanted particle on the wafer surface can come from a number of sources .It can originate from environment, factory personnel, and equipment. Particle once deposited on the surface can lead to the formation of permanent features in the layers being defined in subsequent steps. These undesirable deformations or spot defects do not necessarily have the same shape and size as the original particles. Some time a particle can lead to the killer defect which can kill the IC. An example is shown in figure 1.[3],[5].

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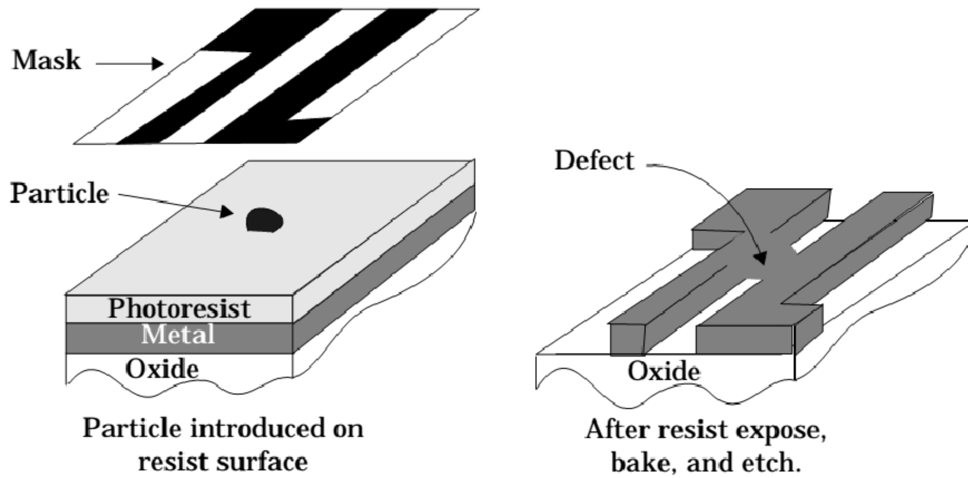

Figure 1: Particle to Defect transformation

3. Optimization of inspection recipe parameter on defect capture rate

Variation in Recipe Parameter was done in this case. At a time 1 parameter was varied in accordance with other two parameters which are kept fixed. Readings were obtained for the best Optimizing value of parameters.[4],[6]. Basically 2 parameters were used in this case:

- Threshold
- Focus offset

Threshold: Range of threshold is 0 to 255 .Default is 30. Each pixel in the difference image that has a grey level above this value is identified as a defective pixel. Lower values increase defect threshold sensitivity. Higher values reduce the number of reported defective pixels.

Focus offset: Default value is 0.0 Set values to optimize site selection.

For optimizing best result species, various iterations were taken by varying threshold and focus offset. Readings were noted for total defects, cluster defects, un-cluster defects and defect density by varying threshold and focus offset. After these iterations graph was plotted between threshold, offset and one parameter i.e. defect count, cluster def. and un-cluster def. one at a time.

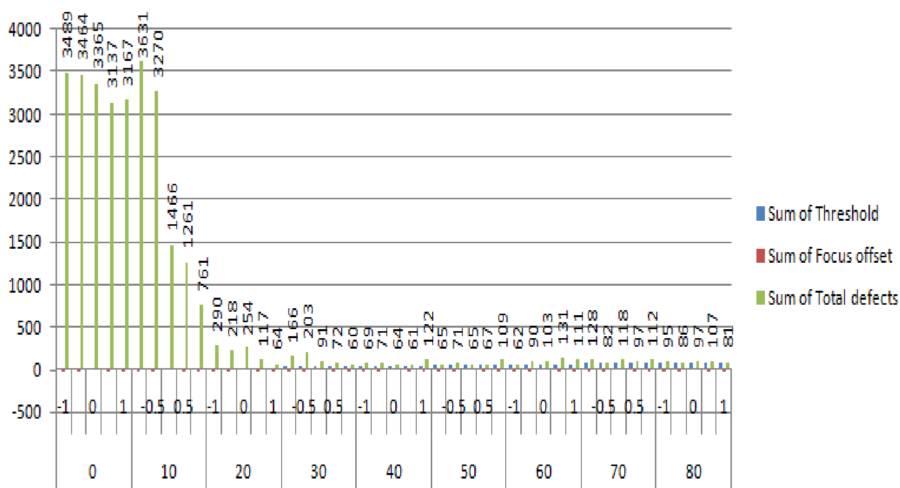

Figure 2 (a): total defect v/s focus offset and Threshold

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Wafer is inspected on Defect Inspection tool by varying threshold from 0 to 80 in step of 10 as shown in figure and focus offset from -1 to +1 in step of 0.5 . A set of 45 readings were taken for defect count, cluster defect, un-cluster defect and defect density. Individual graph is plotted for each i.e. total defects, cluster defects, un-cluster defects and defect density. The graph for total defects v/s threshold and focus offset is shown in figure 2 (a).

From the graph in figure2 (a), (b), (c) it was analyzed that defect count, cluster and un-cluster defects decreases as threshold is increased from 0 to 80.

From the graph in figure2 (d) it was analyzed that variation in Defect density at initial point was not so large, it was somewhat constant but after some time it decreases drastically as threshold increases.

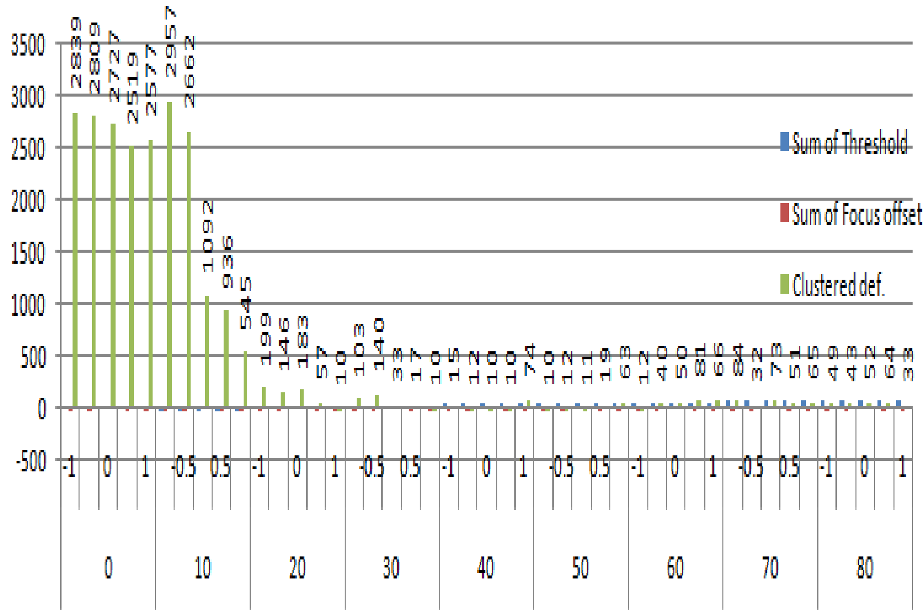

Figure 2 (b): cluster defects v/s focus offset and threshold

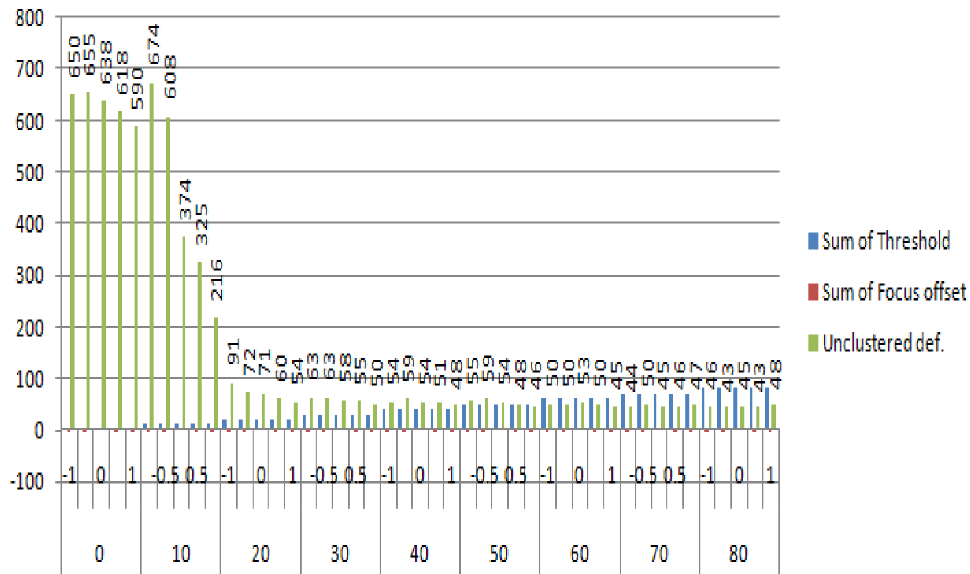

Figure 2 (c): Un-Cluster defects v/s focus offset and threshold

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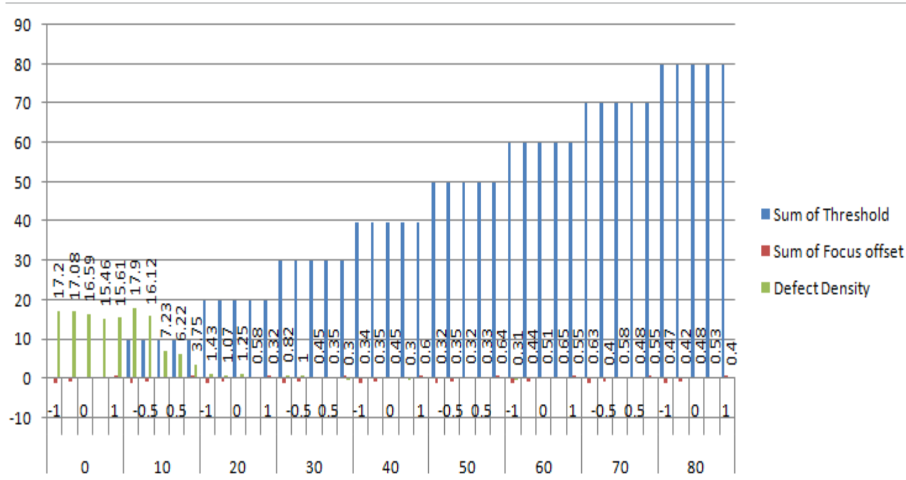

Figure 2 (d): defect density v/s focus offset and threshold

In second case threshold is taken from 12 to 32 and offset focus is fixed at -1 to +1.Again readings were taken for total defects, Cluster defects, un-cluster defects and defect density as shown in figure3.

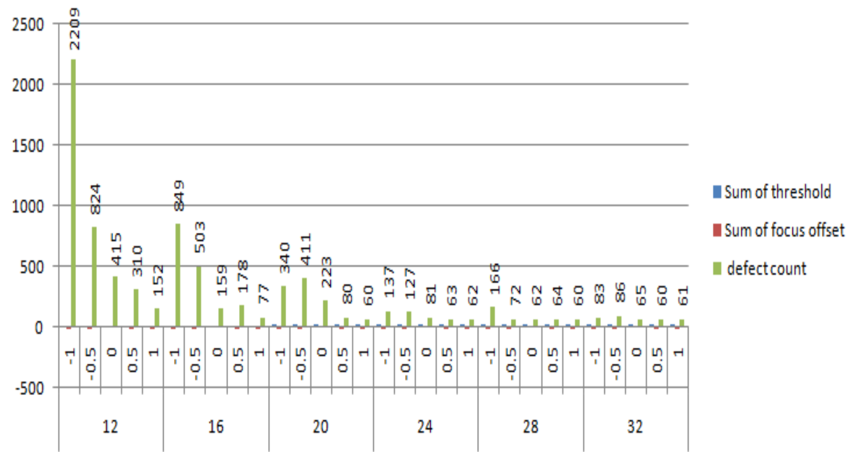

Figure 3 (a): defect count v/s focus offset and threshold

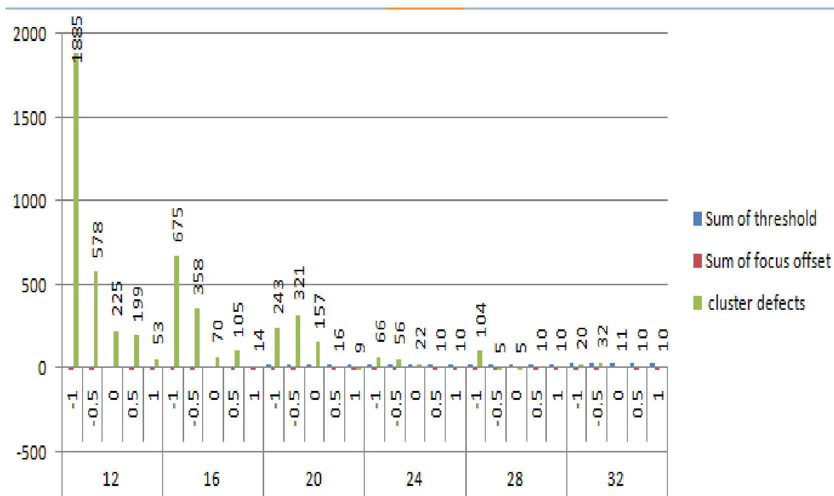

Figure 3 (b): Cluster defects v/s focus offset and threshold

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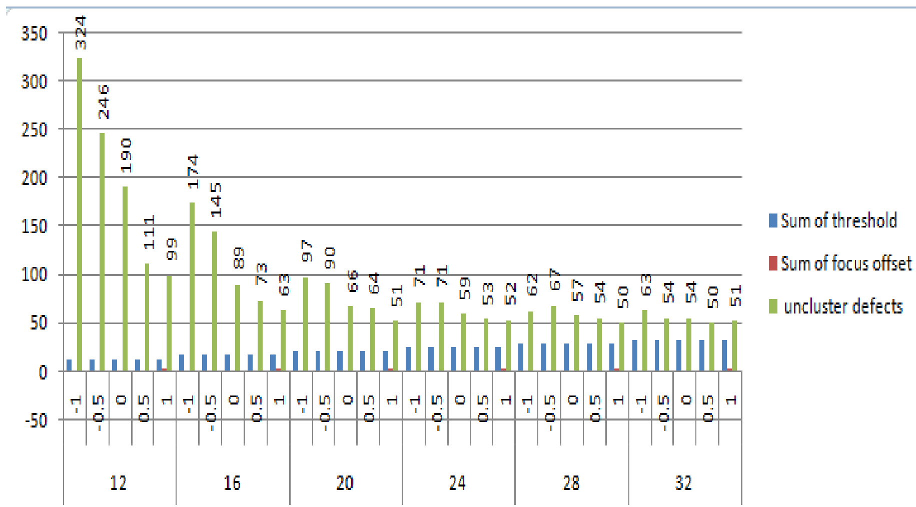

Figure 3 (c): Un-cluster defects v/s focus offset and threshold

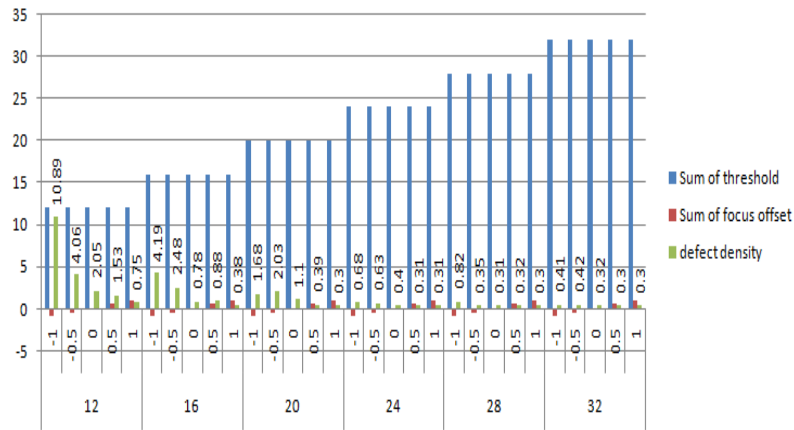

Figure 3 (d): Defect Density v/s focus offset and threshold

In third case the threshold is varied from 36 to 44 in step of 4 and focus offset is kept fixed. Readings were taken for various parameters again and graph is plotted as shown in figure 4.

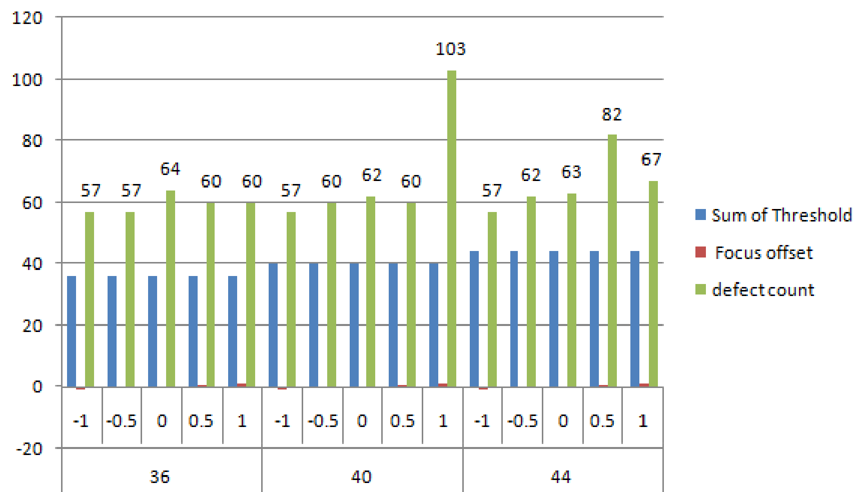

Figure 4 (a): Defect count v/s offset focus and threshold

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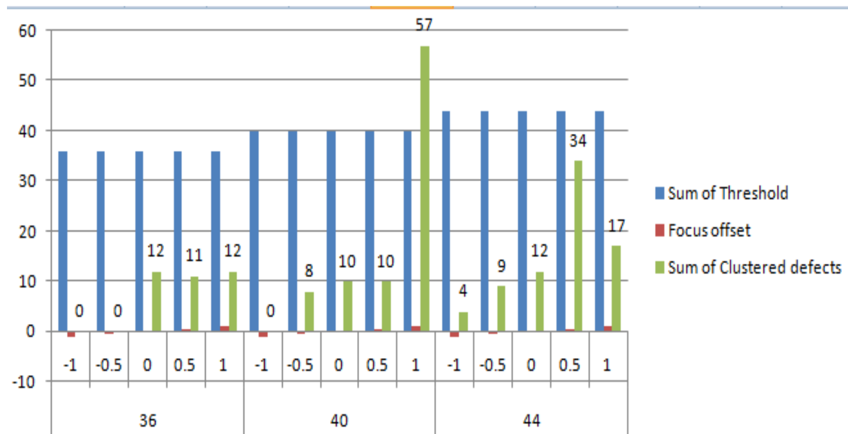

Figure 4 (b): Cluster defects v/s focus offset and threshold

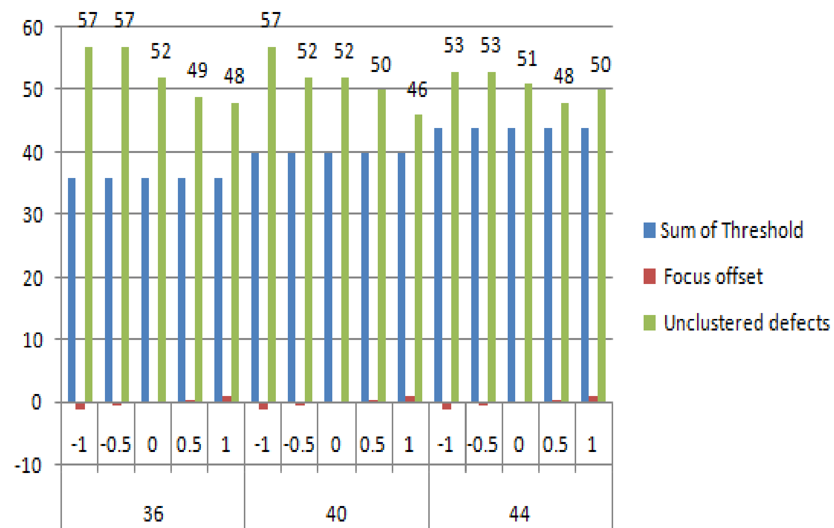

Figure 4 (c): Un-cluster defects v/s focus offset and threshold

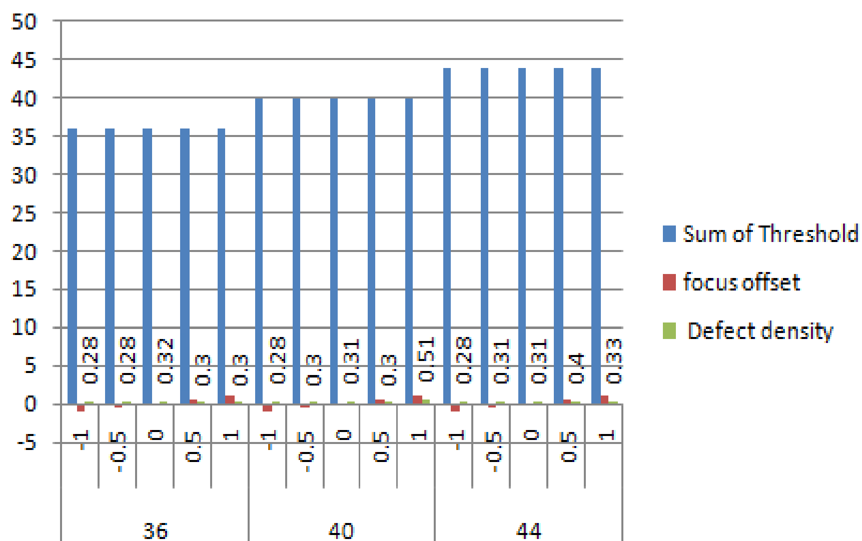

Figure 4 (d): Defect density v/s focus offset and threshold

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Result

On absorbing all the above readings it is concluded that the best optimized species parameter is focus offset at 0.5 micrometer threshold in the range of 20 to 32. The graph is plotted between the real defects and nuiscence defects for each run by inspecting the defects on defect inspection tool.

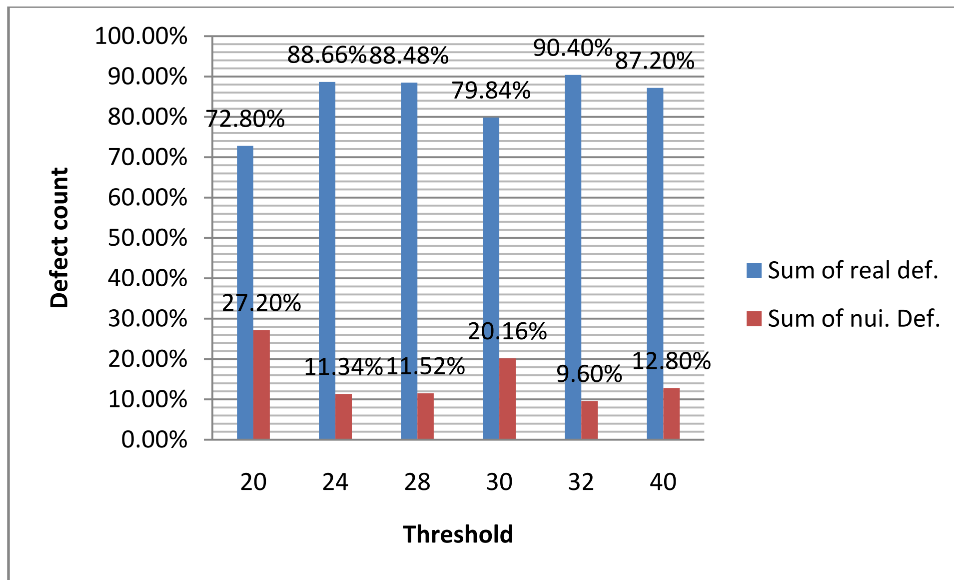

Figure 5: Optimized graph

All the real defects are reviewed on the ORS (Optical Review Station) tool and images are taken. Images of real and nuiscence Defects are shown in figure 6

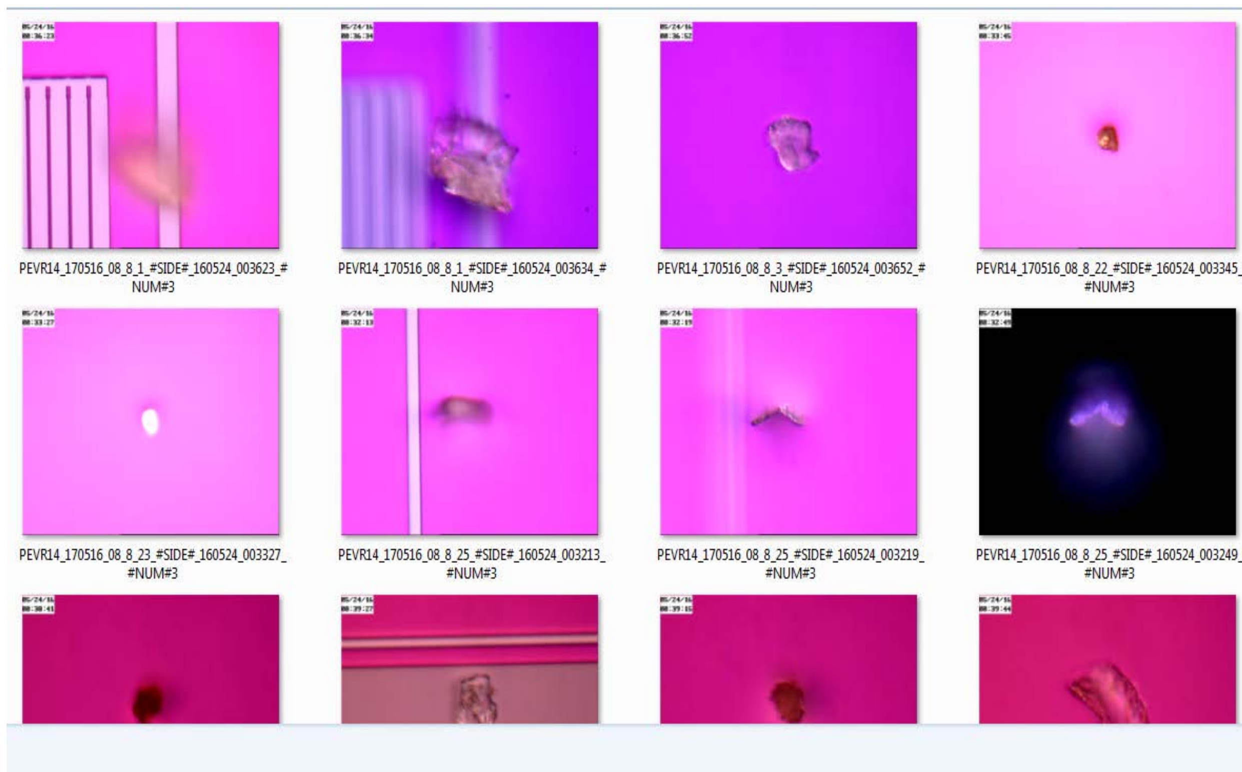

Figure 6 (a): Real Defects on Reviewed on ORS

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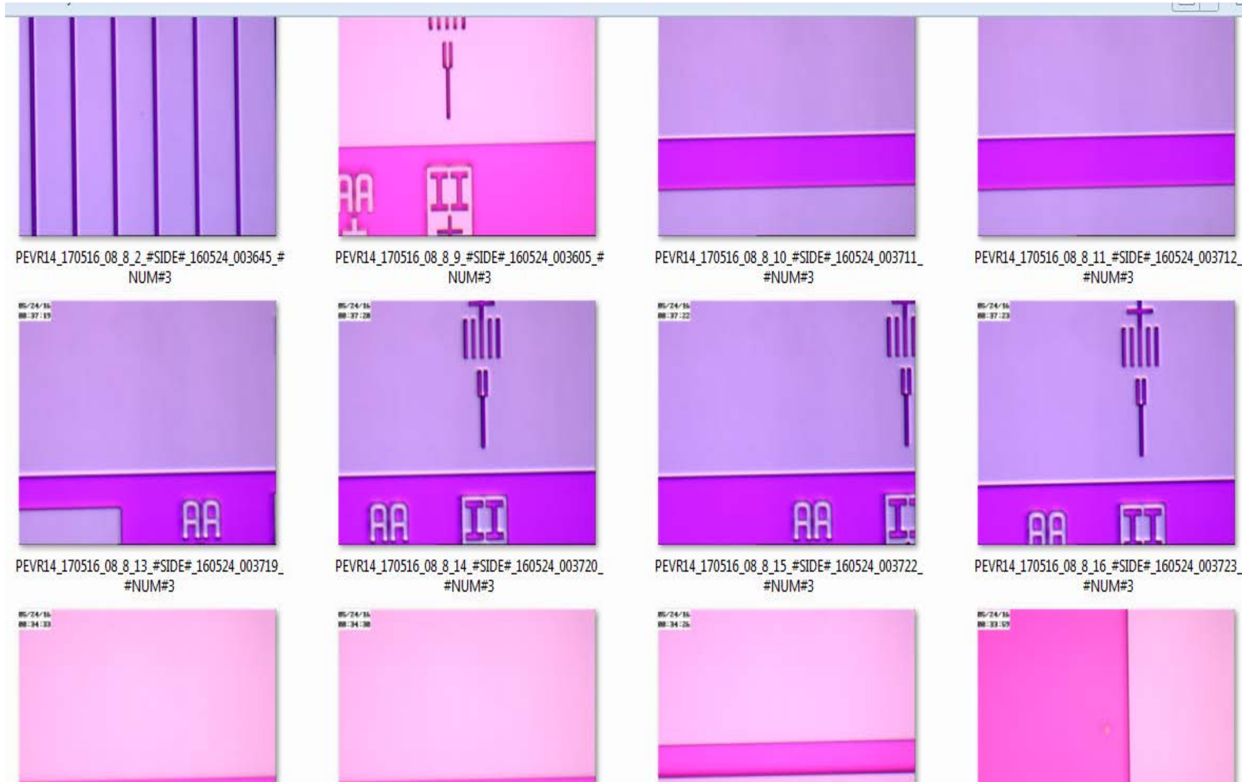

Figure 6 (b): Nuiscence defects reviewed on ORS

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