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A review paper on AN EFFECTIVE FULL ADDER DESIGN using different logic style for low power dissipation

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Abstract

Adders are the key components in building of any digital circuits. They are used not only for addition but also used for multiplication & division too. Adders find a wide application in very large scale integrated circuits like in arithmetic logic circuits to application specific integrated circuits. At the same time, building low-power, high-performance full adder cells is of great interest. The objective of this paper is to give an overview of full adder implementation using various logic styles at 45 nm technology. Logic style is the supreme factor, which influence switching speed, delay & power dissipation. Different logic styles have been compared taking full adder design as a reference & power dissipation as a reference parameter. Simulation results of full adder at a technology of 45 nm have been provided.

Keywords: Full adder, Complementary pass transistor, CMOS, Pass transistor, Transmission gate

Introduction

There are many factors that degraded the performance of integrated circuit(IC) chip. The factor that haunt the performance are cost it includes one – time or fixed charges, verification cost, die cost, bad – die cost, test cost etc., design productivity, fabrication techniques & power consumption. The growing market of battery- powered, portable computing devices such as cellular phone, notebook, and personal computer entail the need of area & power efficient VLSI circuits. That's has driven the VLSI microprocessors to increases their performance. It is very difficult to maintain this performance standard through fabrication techniques only. Enhancements in other domains are mandatory to support the performance standard. An excellent design methodologies and selection of appropriate logic style is equally essential in achieving performance standard. As growing importance of low power, small area & high speed circuitry design methodologies it become popular for wide application in VLSI like in design of microprocessor & system mechanism[1]. Full adder using static or dynamic logic style for minimization of power is one of the prime concerns in today's VLSI design methodologies because of two primary reasons. Firstly, requirement of enlarging the battery life span of portable equipments. Secondly, due to increasing the count of transistor on single chip leads to high power dissipation [2-4].

The whole computational block power consumption can be decreases by implementing low power techniques on full adder circuitry. Full adder is the key component of an ALU. The power consumption of a processor is decreases by decreasing the power consumption of an ALU, and the power consumption of an ALU can be decreases by decreasing the power consumption of Full adder. So the full adder designs with low power dissipation are becoming more popular these days and by enhancing the performance of full adder block automatically increases the performances of overall system. In this paper, implementation of full adder using various logic styles has been discussed and their corresponding results have been concise.

II. LOGIC STYLES

Logic style is the major factor, which influence the performance of the circuit, switching speed, delay & power dissipation. It also has an impact the process, working as well as compatibility of surrounding circuitries. So an excellent design methodologies and selection of appropriate logic style is essential in achieving performance rate.

i) Static Logic Design

In static logic circuits allow versatile implementation of logic functions based on static or steady state. In

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other words all valid gate output at every point in time (except when switching) is connected to either GND or VDD via a low resistance path. Hence it produces the output corresponding to the applied input voltages after a certain time delay, and up hold the output level as long as the power supply is on. This approach, however, has drawback of requirement of a large number of transistors to implement a function and may causes a considerable time delay. Because of this reasons it can't accomplish the high switching speed[5].

ii) Dynamic Logic Design

For high- switching speed, high- performance & high-density digital circuit implementation where reduction of transistor count results in small silicon area & reduction in circuit delay is of major concern. It offers several advantages over static logic circuits. Consequently dynamic logic circuit has a capability of temporary storage of voltage level at the capacitive node of high impedance. In other words Dynamic logic is temporary (transient) in that output levels will remain valid only for a certain period of time. However, power consumption increases with the parasitic capacitances and also due to pre-charging &evaluation mechanisms of charging & discharging of capacitance result in unnecessary power dissipation. Therefore, it is concluded that the Dynamic logic circuit design is used for low power circuit design. Static Logic Style can be classified as Complementary CMOS logic, and Pass Transistor Logic[6].

III. DIFFERENT TYPES OF FULL ADDER

i) Conventional CMOS

The schematic diagram of a conventional CMO Sadder is shown in the given figure1. Signals noted with '-'are basically complementary signals. The width of the transistors is increased to obtain a reasonable conducting current to drive the capacitive loads which further results in increased capacitance and high propagation delay[7][5].

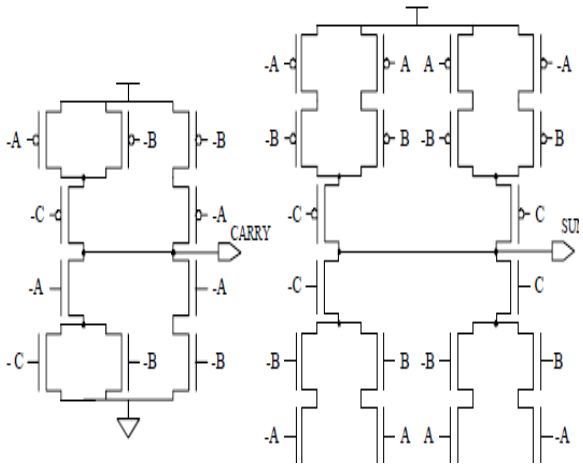

Figure 1: Schematic view of CMOS FA

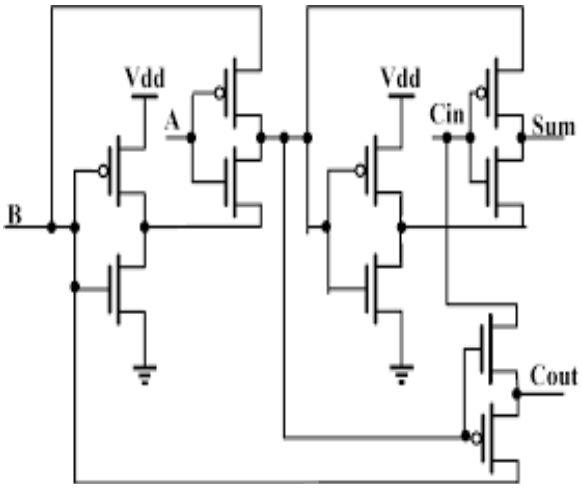

Figure 2: Schematic view of 10-Transistor CMOS FA[14].

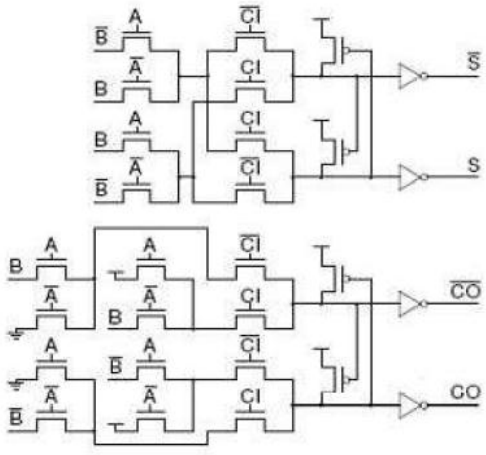

Figure 3: Schematic View of 28-T CPL FA[14].

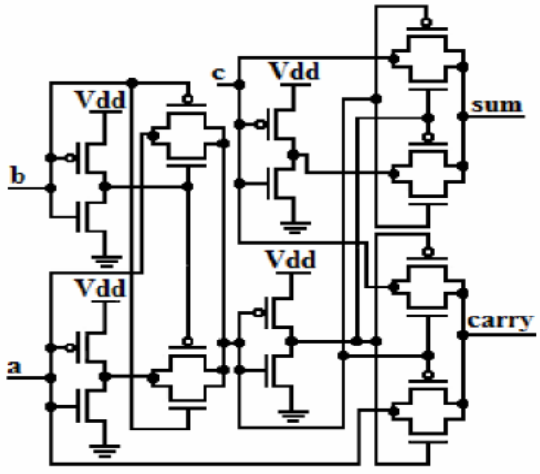

Figure 4: Transmission Gate Full Adder 20-T[14].

The basic advantage of 10T full adders is smaller area and lower power utilization. It becomes more not easy and even obsolete to keep full output voltage swing operation as the design with fewer transistor count and lower power utilization are pursued. In pass transistor logic the output voltage swing may be degraded due to the threshold voltage defeat problem. The reduction in voltage swing leads to lower power consumption but may also lead to slow switching in the case of cascaded operation such as ripple carry adder. A low VDD operation the corrupted output may even cause break down of circuit. The smallest voltage that 10 T adder can work at 0.7V. The excessive power dissipation and long delay are attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full-swing transitions. The elimination of the path to the ground reduces the total power use by reducing the short circuit power [8].

ii) Pass transistor logic

The major difference between the CMOS logic style and the pass-transistor logic style is that the source side of the logic transistor network in pass transistor is connected to some input signals instead of the power lines. The advantage of pass-transistor logic network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors, decreases the input load and eliminate the Vdd to gnd paths[9][10]. The realization of logic function in pass-transistor network result in smaller area i.e., area savings and higher operating speed when compared with the corresponding gate logic realization[11]and it is used for low power applications.

a) Complementary pass transistor logic

A CPLgate [12][13] consists of two NMOS logic networks (one for each signal rail), two small pull-up PMOS transistors for swing restoration, and two output inverters for the complementary output signals [9]. In CPL, the logic functions are implemented by the use of only an NMOS. This basically results in low input capacitance and high speed operation.CPL circuits consume less power than conventional static logic circuits because the logic output voltage swing of the pass transistor is less than the supply voltage level[6].

iii) Transmission Gate Full Adder

A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The transmission gate consists of two MOSFETs, one n-channel responsible for correct transmission of logic zeros, and one p-channel, responsible for correct transmission of logic ones. A transmission gate has three inputs, called source, n-gate,and p-gate; and it has one output, called drain[14].

IV. CONCLUSION

S. No.	Adder cell	No. of transistor	Supply (V)	Power (µW)	Delay (ns)	PDP (fJ)
1	CMOS	10	0.5	64.81	29.17	1890.50
			0.9	41.61	11.31	470.60
			1	18.40	0.1108	2.04
2	CPL	38	1	0.2729	0.05911	0.02
3	TGA	20	1	0.2008	0.05551	0.01

Table 1: Comparison of various parameters of full-adder at 45nm technology using different logic styles[1][14].

In this paper we compared the performance of CMOS full adder circuit, pass transistor full adder, transmission gate full adder using 45 nm technology. The performance of various full adders given in Table-1 shows that different adders have different

parameter values. No single adder has less delay, power and PDP. So, there is a trade-off between these parameters. The results help us to choose an adder which can give us desired result according to a specific application.

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