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16-BIT CARRY SELECT ADDER

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Abstract

Adders are an electronic circuit which adds the addend, augends numbers with or without previous carry generated and provides the summations and carries as a result. The adder differs in the type of inputs considered and algorithm used for example Binary, BCD, Excess-3, Hexadecimal adders etc. The 1's complement method, 2's complement method, signed arithmetic etc. The adders widely used in ADCs, digital voltmeters, CPUs of microprocessors, micro-controllers. It also extensively used calculating the memory addresses, table indices, and offsets. Binary adders are the most commonly used adders in which 2'scomplement or1'scomplement is used to represent negative number. Another approach of adder design includes low power module, high speed, large bandwidths or channels. Numerous adders are designed by making tradeoffs between power, propagation delay and size. In most of the digital adders, speed of addition is limited by the time required to transmit a carry through the adder. Carry Select Adder (CSlA) is one of the fastest adders fabricated with data-processing processors to perform fast arithmetic operations. This paper presents a review on CSlA.

Keywords: *ADCs, RCA, Delay, LSB, CSkA, CSlA,*

Introduction

The modern era becomes entirely dependent on electronic devices. Where most of the electronic devices from clinical instruments to machines used for exercise by physiotherapist, wave meter, power meter, calculator used by a shopkeeper to the processors and microcontrollers used in computer system, mobile phones, PDAs etc. all uses a binary adder. Therefore, it attracts the researchers and educators for research. There are a variety of adders and each has certain performances. The selection of adder is based entirely on needs of the operations. For high speed arithmetic operation carry select adder is widely used.

Half adder

The half adder is an example of a simple and basic, functional digital circuit built from two logic gates an XOR gate and an AND gate. The half adder adds to one-bit binary numbers say A and B. The outputs are sum (S) and carry (C). The figure 1 shows a logic circuit of a half adder [1] and table 1 represents the truth table [2] for corresponding logical states of operations.

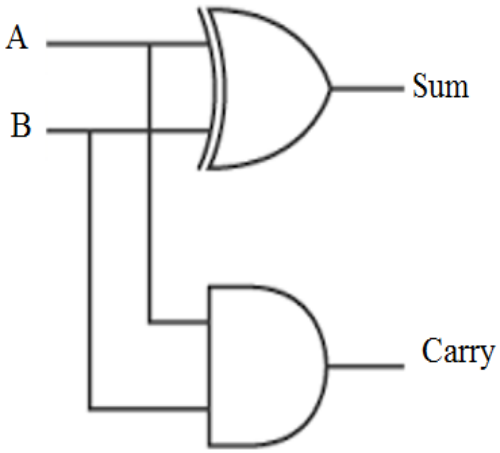

Figure 1: Halfadder

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Table 1: Truth table of half adder

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder

A full adder adds binary addends, augends and accounts for the values carried in as well. A one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and C_{in}; which represent the addend, augends, and carry input. C_{in} is a bit carried in from the previous less significant stage. The circuit produces a two-bit output, Sum (S) and Carry (C_{out})**.**It is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. Whereas the equation of the sum and carry is

Sum = A XOR B; ---------- (1)

Carry = A AND B; ---------- (2)

The figure 1 shows a logic circuit of a half adder [3] and table 1[4] represents truth table for corresponding logical states of operations.

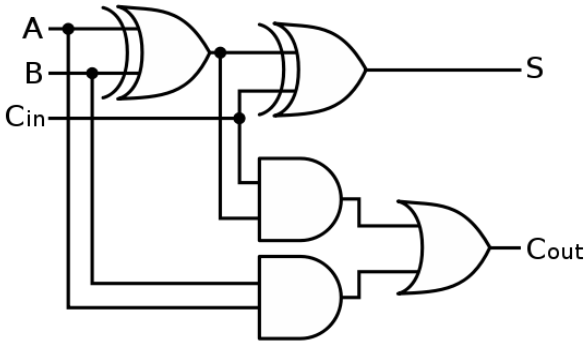

Figure 2: Logic Circuit diagram of fulladder

Table 2 Truth table of full adder

X	Y	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Ripple Carry Adder

Arithmetic operations like additi1on, subtraction, multiplication, division are basic operations to be implemented in digital computer using basic gates. The adder circuit itself able to perform other operations of subtraction, multiplication and division by introduction of a small control logic circuit. An N-bit binary adder can be constructed using N full adders. In which each full adder inputs a carry forwarded by previous (LSB) carry output. This kind of adder is a known as Ripple Carry Adder (RCA), since each carry bits "ripples" to the next full adder. The first full adder may be replaced by the half adder. Figure 3[5] shows a 4-bit logical circuit of ripple carry adder.

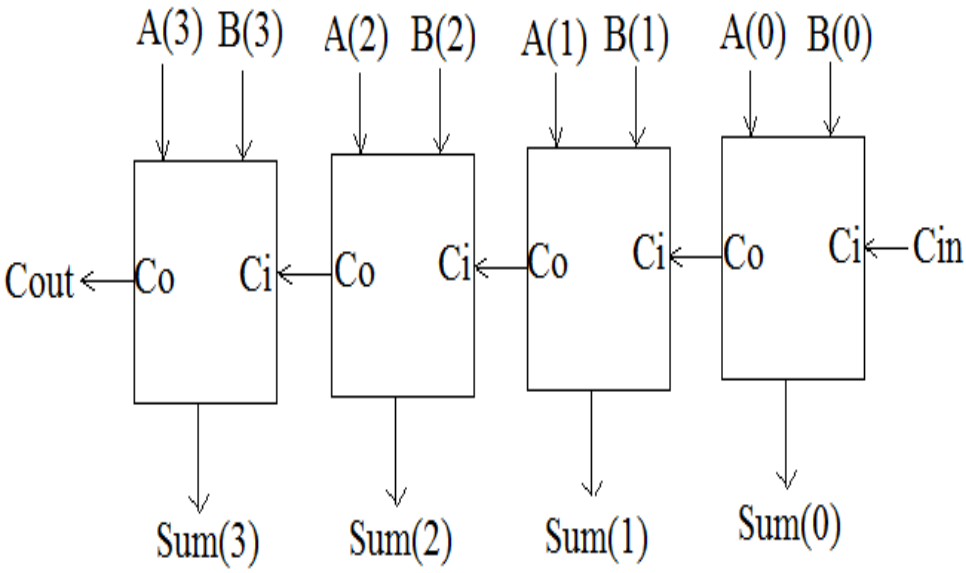

Figure 3: Ripple carry adder

It is visible from the logical circuit diagram that carry generated at very first stage (LSB) propagated sequentially to the last stage (MSB) of the circuit and hence produce a large delay for the operation.

Carry Skip Adder

A carry-skip adder (also known as a carry-bypass adder) is another adder implementation that improves on the delay of a ripple carry adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders to form a block-carry-skip adder.

In Carry Skip Adder, a long chain of RPC is broken into number of groups. A carry skip chain defines the distribution of ripple carry blocks, which compose the skip carry blocks, which further compose the skip adder. Skip Carry Adder are divided into blocks, where a special circuit detects quickly if all the bits to be added are different (Pi=1intheentireblock). The carry skip adder provides a compromise between a ripple carry adder and a CLA. The carry skip adder divides the words to be added into blocks. The signal produced by this circuit will be called block. This method reduces propagation delay to a particular extent only if the word length is large. The circuit diagram of carry skip adder is shown in figure 4[6].

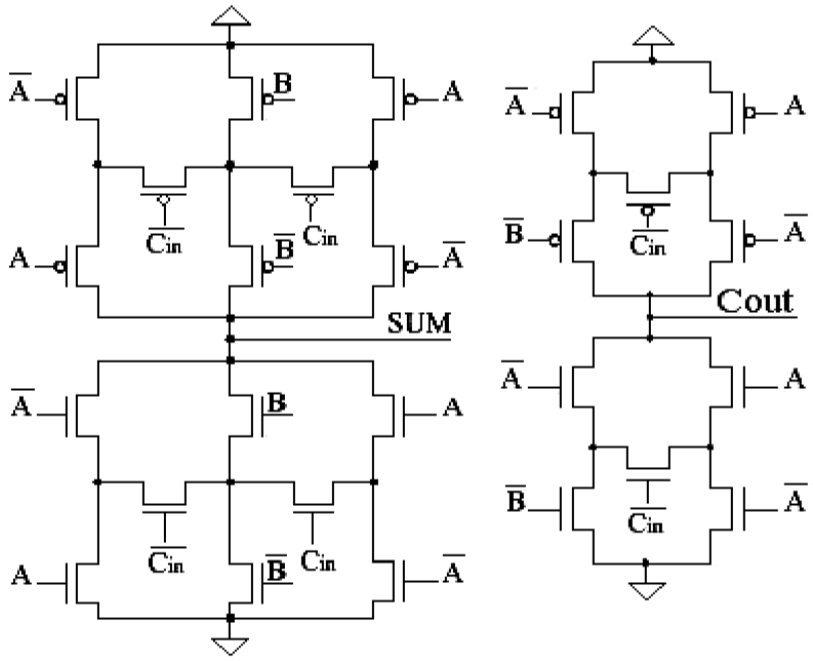

Figure 4 Carry Skip Adder

Carry Select Adder

A Carry Select Adder is a particular way to implement an adder, which is a logic element that computes the (n+1) bits sum of two n-bit numbers. The carry-select adder is simple but rather fast. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders(therefore two ripple carry adders)in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The logic diagram of "16-Bit Carry Select Adder" is shown in figure 5[7].

16-Bit Carry Select Adder

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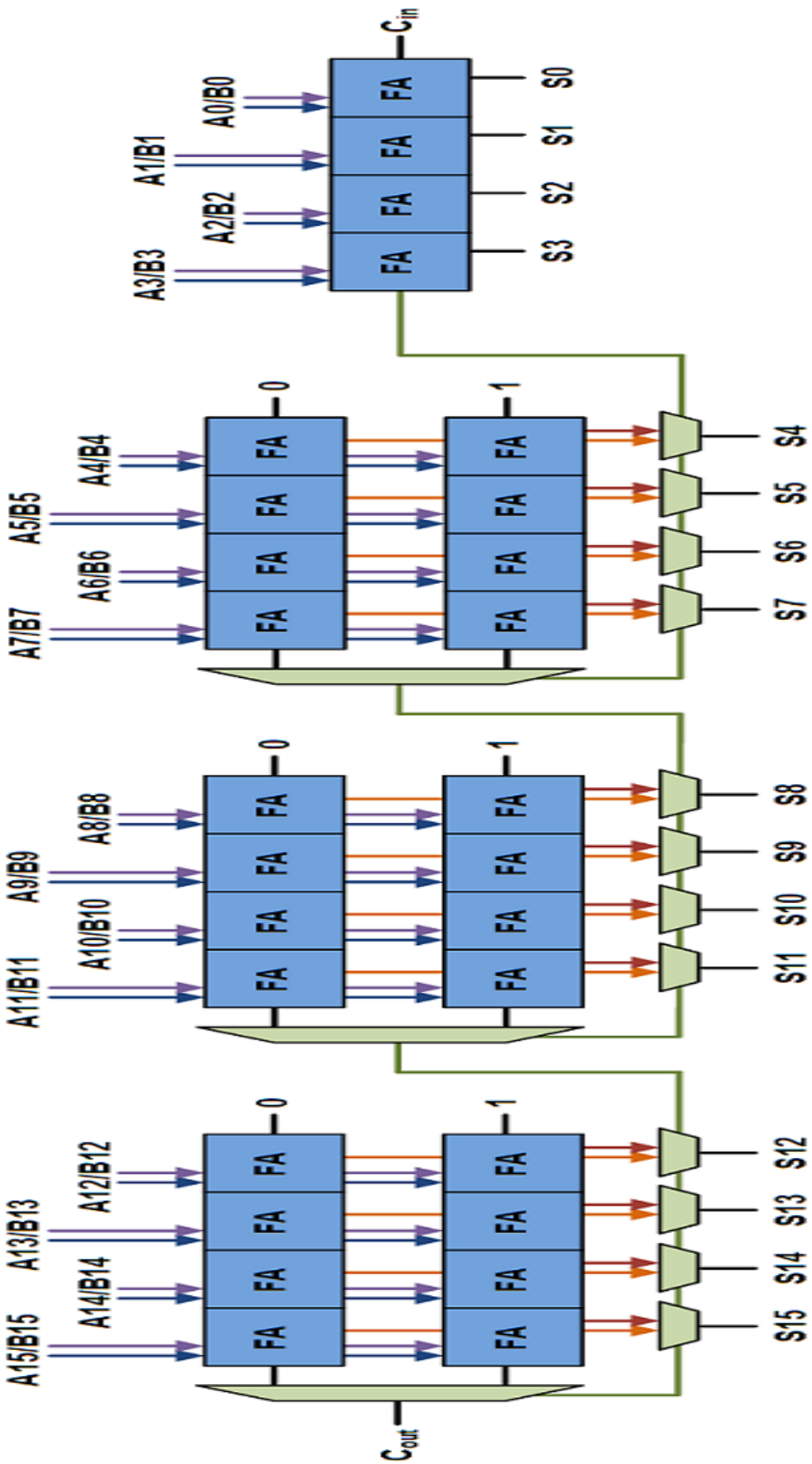

Figure 5Logic Diagram of 16-Bit Carry Select Adder

Results & Conclusion

The performances of adder topologies are studied against area, delay and power dissipation. At 500MHz, power dissipation and area i.e. gate count for RCA, CSkA, and CSA are in increasing order while it is found that the delay for the topologies are in decreasing order and minimum for CSA.

Table 3: Comparison of Power, Delay and Area of RCA, CSkA, and CSlA

Adder	Power(mW)	Delay(nS)	Area (Gate Count)
RCA	0.206	4.208	288
CSkA	0.603	3.622	388
CSlA	1.109	2.78	600

References

1. Digital logic and computer design by M. morrismano(2nd edition)
2. Y. Sunil Gavaskar Reddy, V.V.G.S. Rajendra Prasad, "Power Comparison of CMOS and Adiabatic Full Adder Circuits", International Journal of VLSI design & Communication Systems (VLSICS), Vol. 2, No. 3, September 2011.
3. Digital Electronics by Salivahanan
4. Shubin.V.V,"Analysis and Comparison of Ripple Carry Full Adders by Speed", Micro/Nano Technologies and Electron Devices (EDM), 2010, International Conference and Seminar on, pp. 132- 135, 2010.IEEE transactions on, Vol. 11, Issue 1, pp. 105-119, 2012.
5. Design and Implementation of 16-Bit Carry Skip Adder using Efficient Low Power High Performance Full Adders, ERCICA-2014, DOI: 10.13140/2.1.3303.9045
6. RomanaYousuf, Najeeb-ud-din,"Synthesis of Carry Select Adder in 65 nm FPGA", IEEE.
7. Sarabdeep Singh, DilipKumar,"Design of Area and Power Efficient Modified Carry Select Adder", International Journal of Computer Applications, Vol. 33, No. 3, pp. 14-18, Nov 2011.